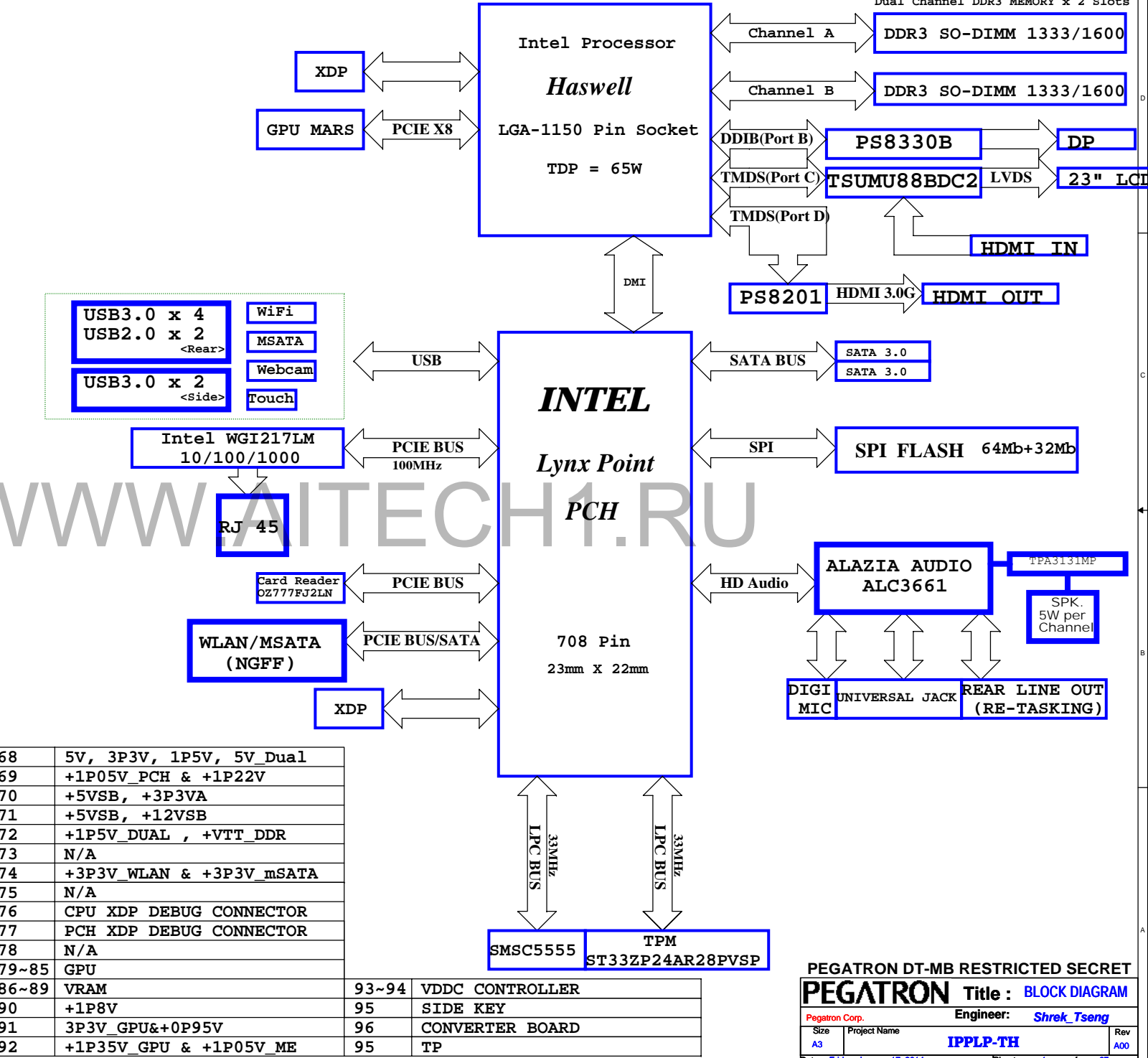
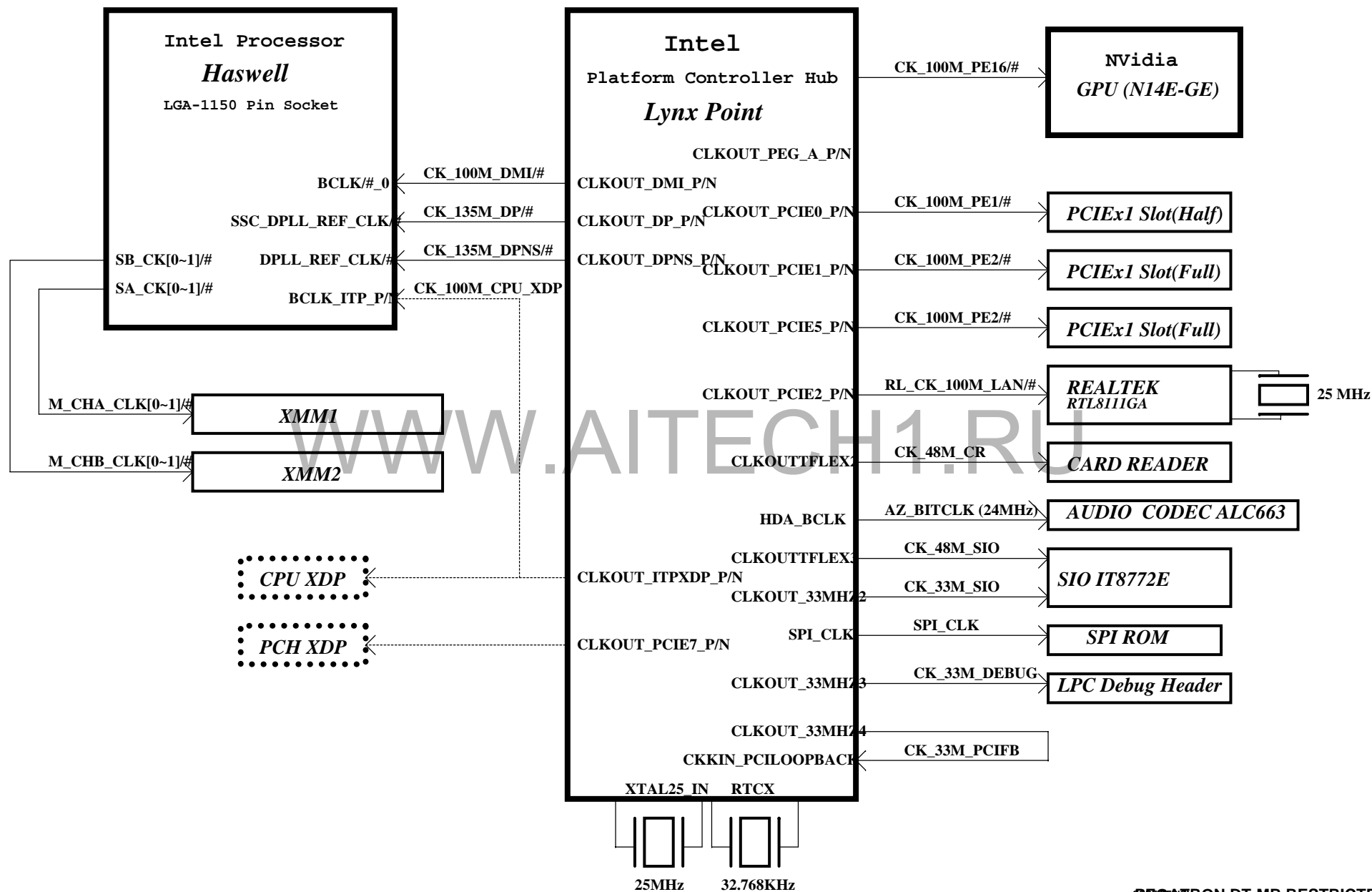


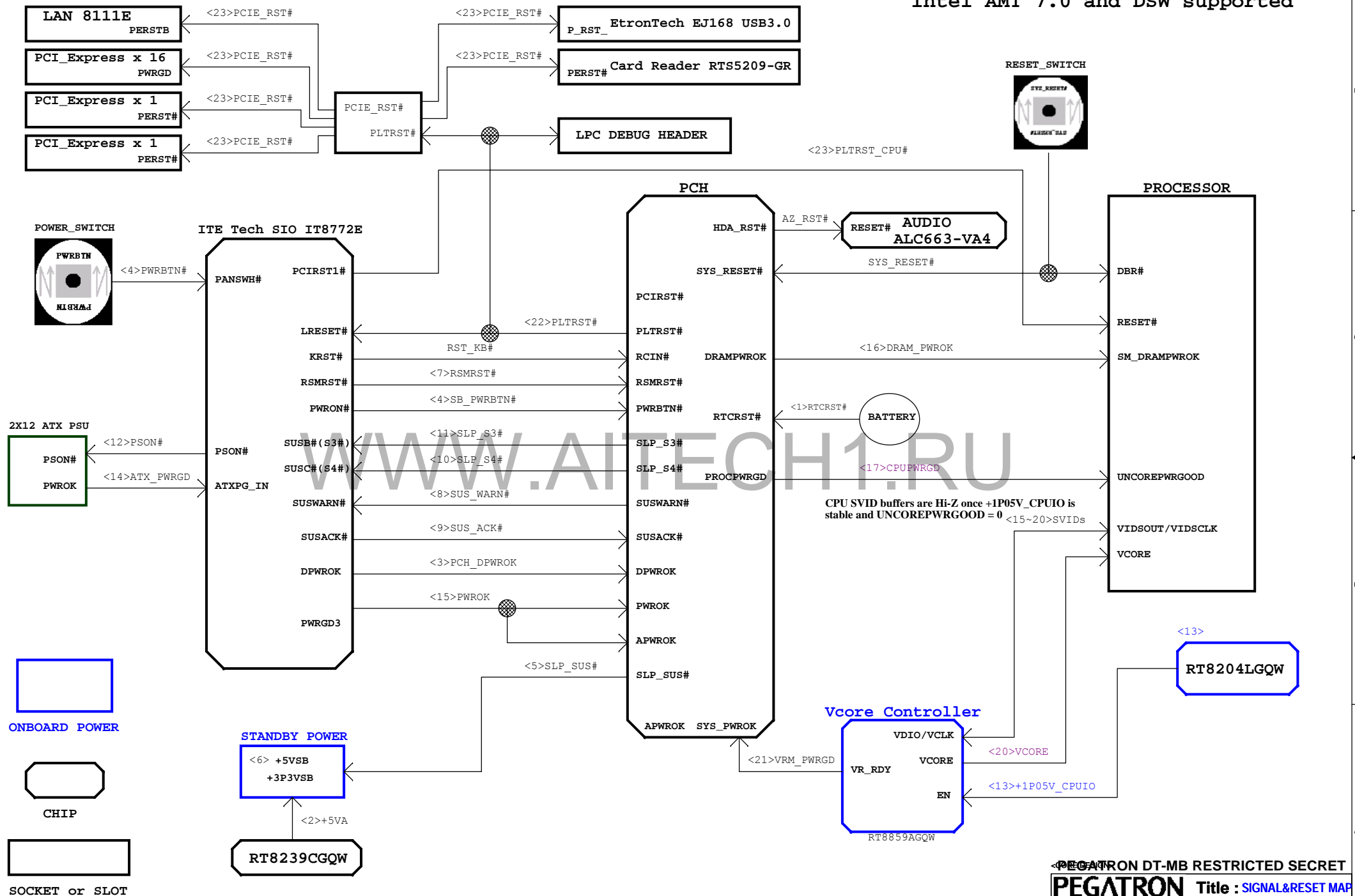
IPPLP-RH

PAGE	TITLE
01	BLOCK DIAGRAM
02	CLOCKS DISTRIBUTION
03	SIGNAL & RESET MAP
04	CHANGE HISTORY
05	POWER FLOW
06	POWER DISTRIBUTION
07	POWER SEQUENCE
08~13	Haswell LGA-1150
14	VGA DEBUG
15~16	DDR3 CHANNEL A&B
17	DDR3 TERMINATION A&B
18	N/A
19~24	INTEL_PCH(1~6)
25	N/A
26	SM BUS & SPI ROM
27	ME DISABLE
28	MINI-PCIE SLOT-1(WLAN)
29	MINI-PCIE SLOT-3(mSATA)
30	CARD READER
31	INTEL CLARKVILLE
32	LAN JACK
33	SIDE USB3.0 PORT
34	REAR USB3.0 PORT
35	REAR USB3.0 PORT
36	REAR USB2.0 PORT
37	TOUCH & WEBCAM
38	N/A
39	SATA CONN
40	AUDIO CODEC ALC3661
41	AMP
42	REAR LINE OUT& GHS CONNECTOR
43	N/A
44	SIO SMSC5555
45	N/A
46	SCREW HOLE
47	FAN CIRCUIT
48	COM PORT
49	DEBUG LED
50	APS/LPC DEBUG
51~52	SCALAR_TSUMU88BDC2
53	LVDS & CONVERTER CONN
54	SCALAR LCD ENABLE
55	FRONT PANEL
56	HDMI IN
57	HDMI LEVEL SHIFT
58	HDMI OUT
59	G-SENSOR
60	DP REDRIVER
61	DP CONN
62	TPM
63	DC IN
64~66	VCORE CONTROLLER
67	3P3_LAN,12V,1P5V_PCH,3P3V_BG

Revision: B00







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A

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[illegible]

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BBOTQ - BBOTQ Phase Only

VP = Virtual Part.

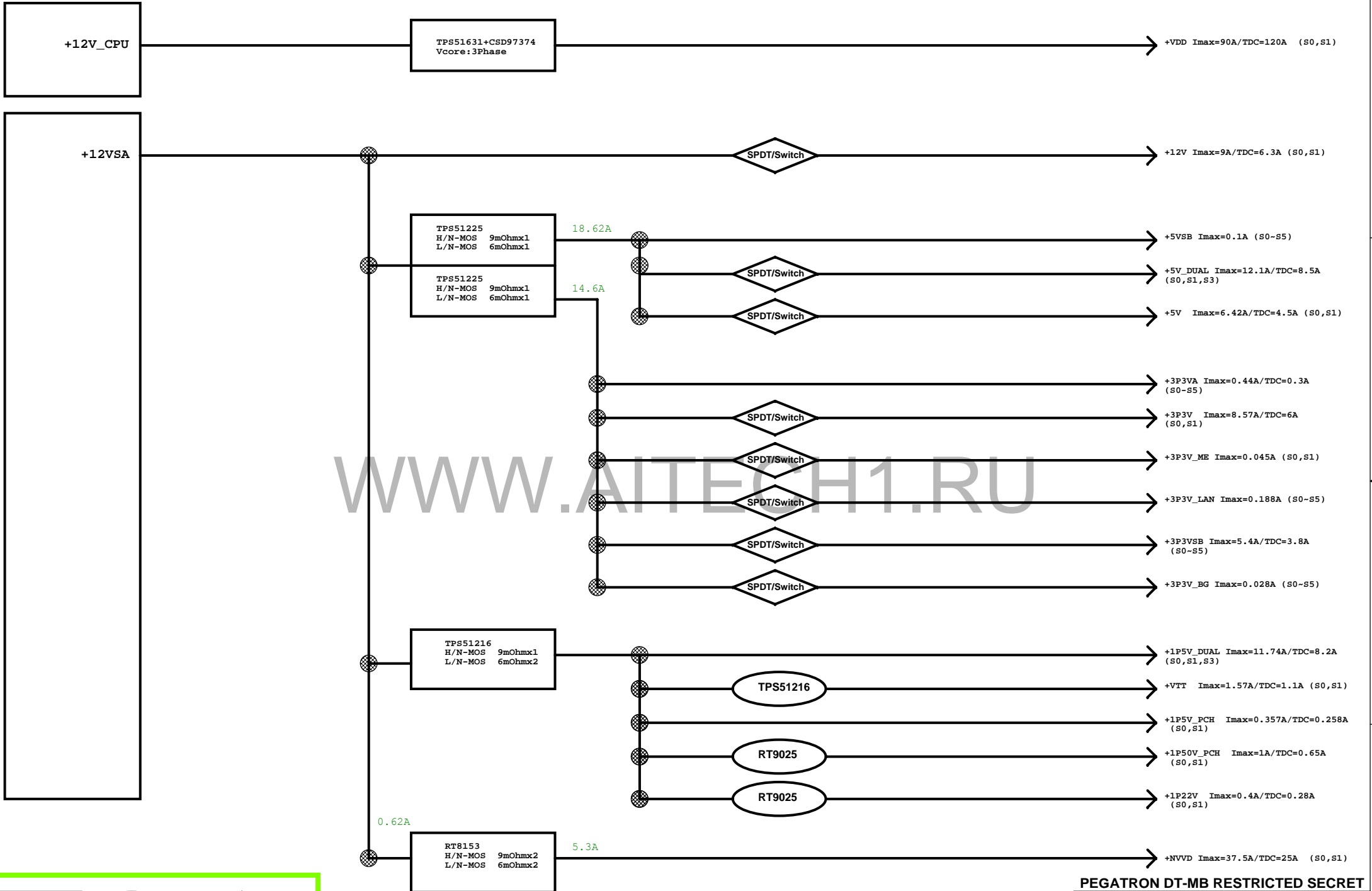
~~DECLASSIFICATION~~ DT-MB RESTRICTED SECRET

PEGATRON Title : **CHANGE HISTORY**

Register.Com Engineer: **Shrek Tseng**

Size	Project Name	Rev
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A3	IPPLP-TH	A00
Date: Friday, January 17, 2014		Sheet 4 of 97



Switching

Linear

SPDT/Switch

	CPU Sandy Bridge
+VCORE	-> 95A (TDC) - 65W
VDDQ	-> 4.2A (I _{max}) - W
VCCST	-> 300mA (I _{max}) - W

	PCH Lynx Point
+1P05V_PCH	-> 1.312A (VCC) - W
+1P05V_PCH	-> 0.306A (VCCCLK) - W
+1P05V_PCH	-> 3.629A (VCCIO) - W
+1V_CPU2PCH	-> 0.004A (V_PROC_I0) - W
+1P05V_ME	-> 0.67A (VCCASW) - W
+1P5V_PCH	-> 0.183A (VCCVRM) - W
+1P5V_PCH	-> 0.07A (VCCDAC1_5) - W
+3P3V_BG	-> 0.0133A (VCC3_3) - W
+3P3V	-> 0.133A (VCC3_3) - W
+3P3V	-> 0.055A (VCCCLK3_3) - W
+3P3V_ME	-> 0.022A (VCCSPI) - W
+3P3VSB	-> 0.261A (VCCSUS3_3) - W
	-> 0.01 (VCCSUSHDA) A - W
+3P3VA	-> 0.015A (VCCDSW3_3) - W
+BATT	RTC (G3) -> 6uA - 0.0198mW

	PCI Express x 1
+12V	-> 5A - 60W
+3P3V	-> 3A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 16
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	REALTEK 8111FA
+3P3VSB	-> 70mA - 231mW
+1P05V_LAN	-> 300mA - 315mW

	SIO IT8772E
+3P3V	-> 200mA - mW

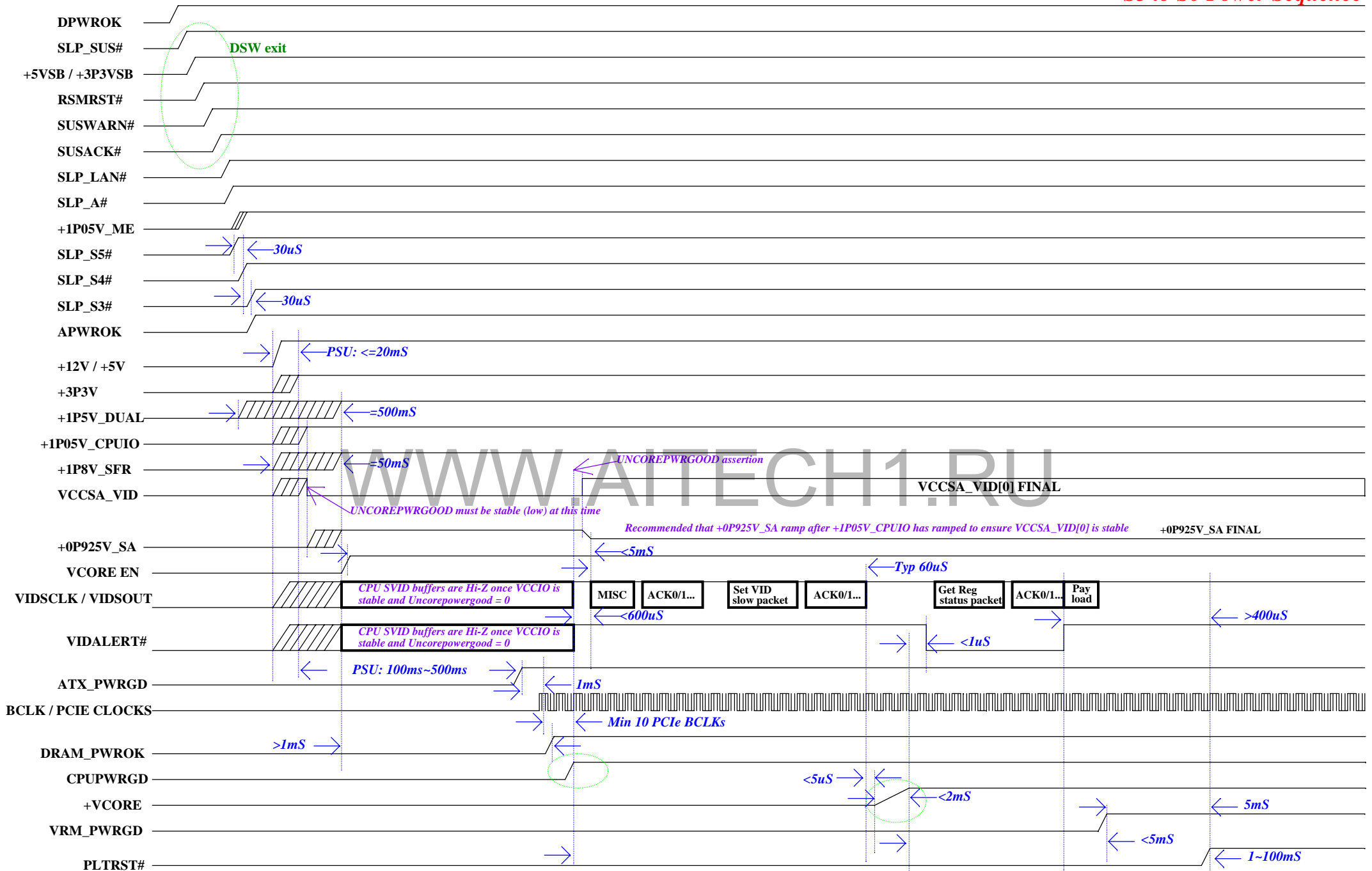
	ALC663 Codec
+5VSB	-> 45mA - 225mW
+3P3V	-> 25mA - 82.5mW

	USB 12 PORTS
+5V_DUAL_B/F	Rear (USB3*4) -> 4A - 20W Front (USB3*1 USB2*1) -> 2.5A - 12.5W Internal (USB2) -> 3A - 15W

	HDMI
+5V	-> mA - mW -> mA - mW

	FANS
+12V	-> 1.2A - 14.4W

	SPI
+3P3V_ME	-> 40mA - 132mW



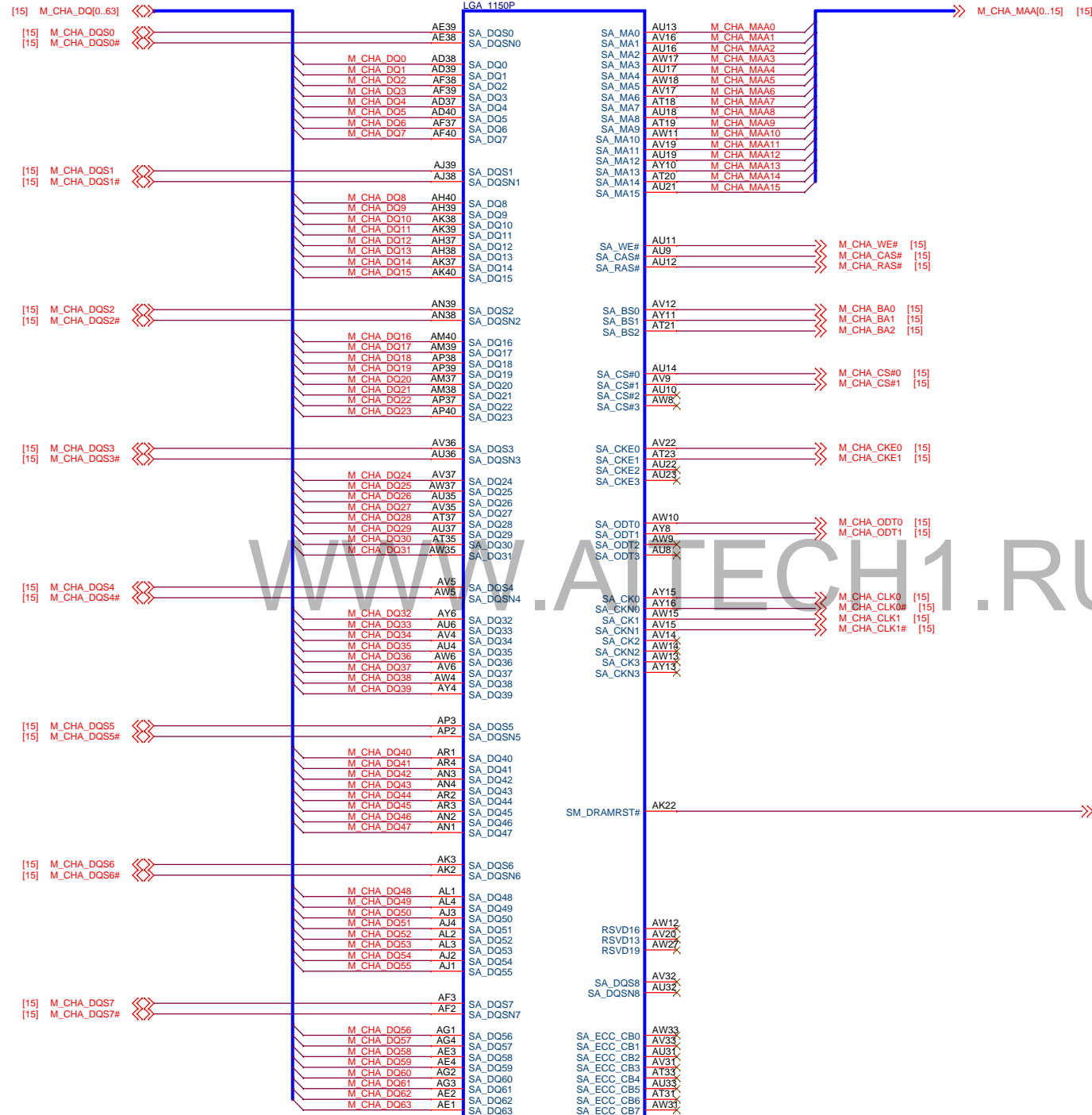
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : POWER SEQUENCE

Pegatron Corp. Engineer: Shrek Tseng

Size A3 Project Name IPPLP-TH Rev A00

Date: Friday, January 17, 2014 Sheet 7 of 97



DDR3_A

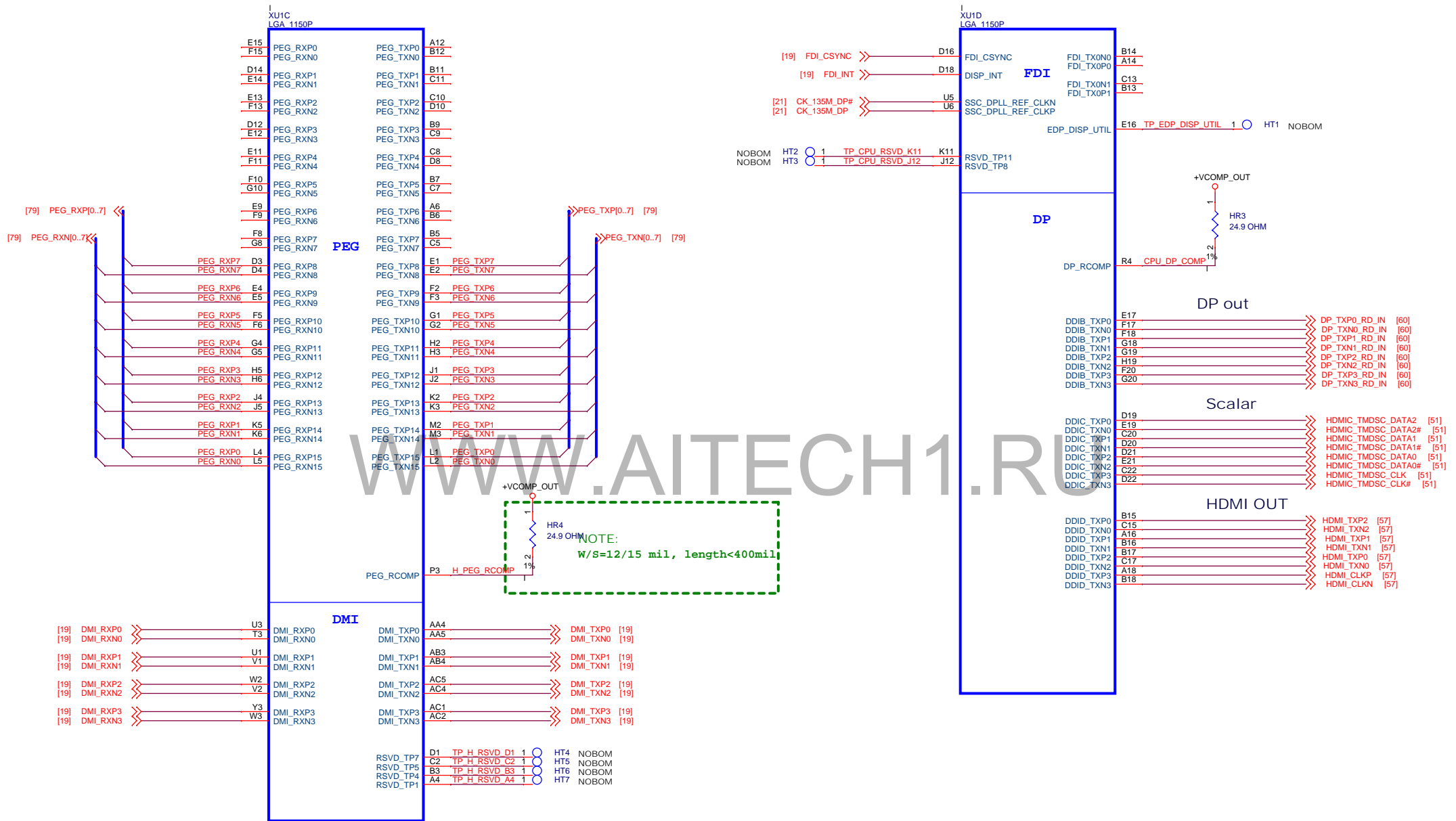
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **DDR3_A 1-6**

Pegatron Corp. Engineer: **Shrek Tseng**

Size	Project Name	Rev
A3	IPPLP-TH	A00

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIE/DMI/DP 3-6

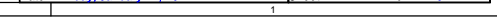
Pegatron Corp. Engineer: Shrek Tseng

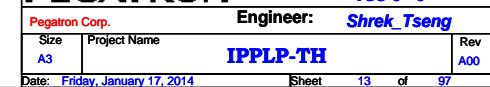
Size A3 Project Name IPPLP-TH Rev A00

Date: Friday, January 17, 2014 Sheet 10 of 97

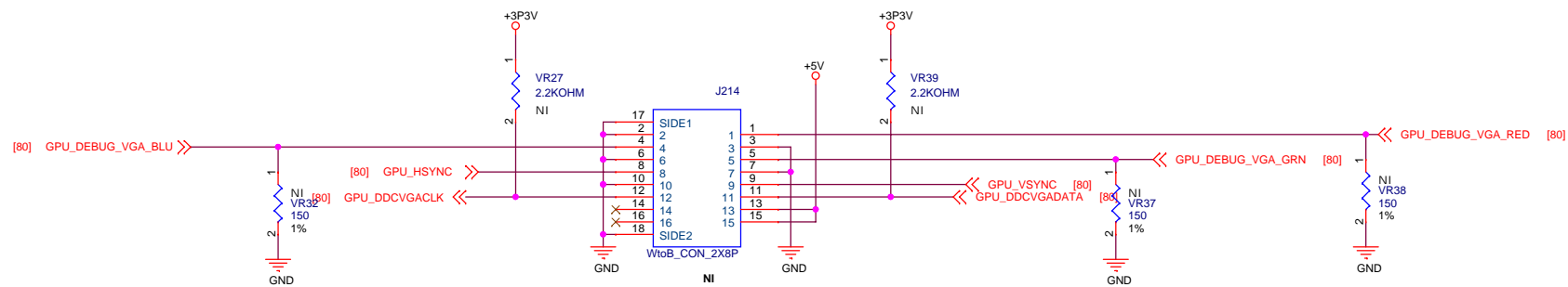
Date: Friday, January 17, 2014

Sheet	11	of	97
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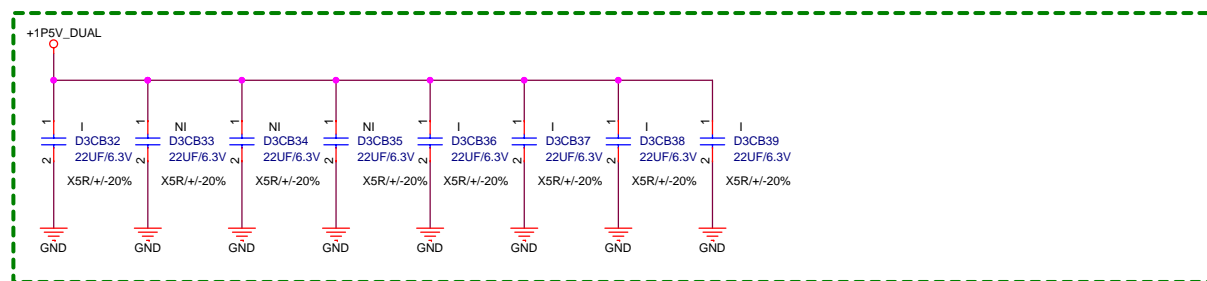
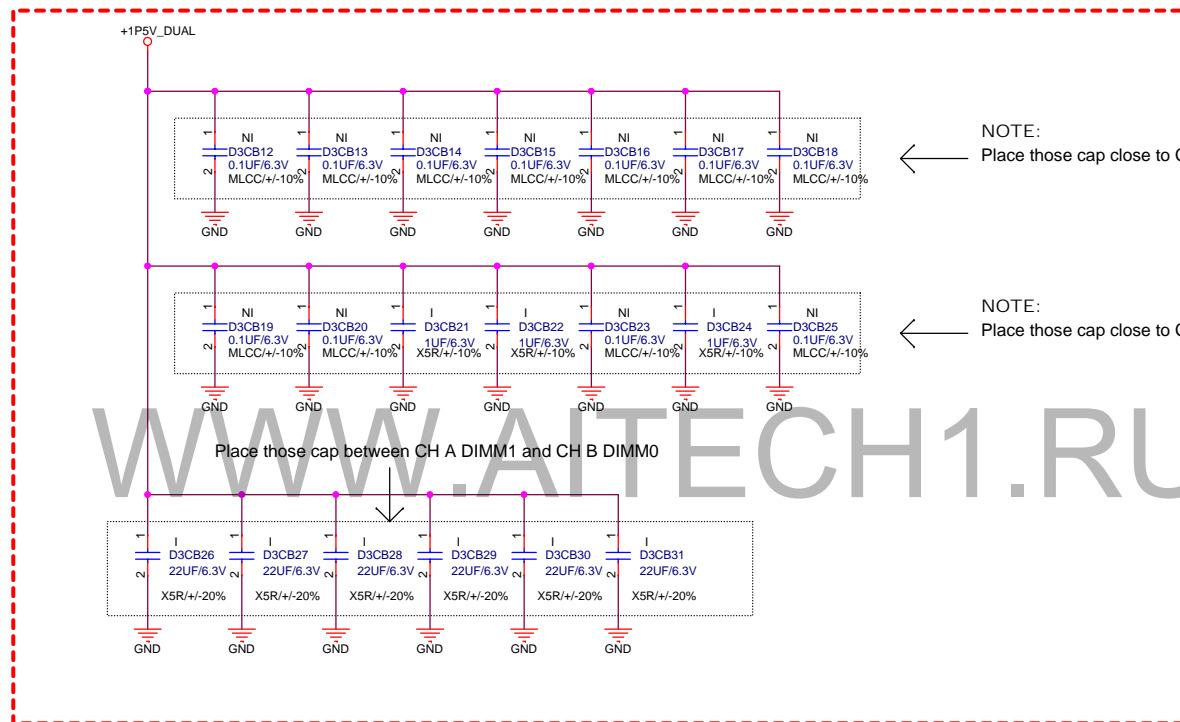
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **VGA DEBUG**

Pegatron Corp. Engineer: **Shrek_Tseng**

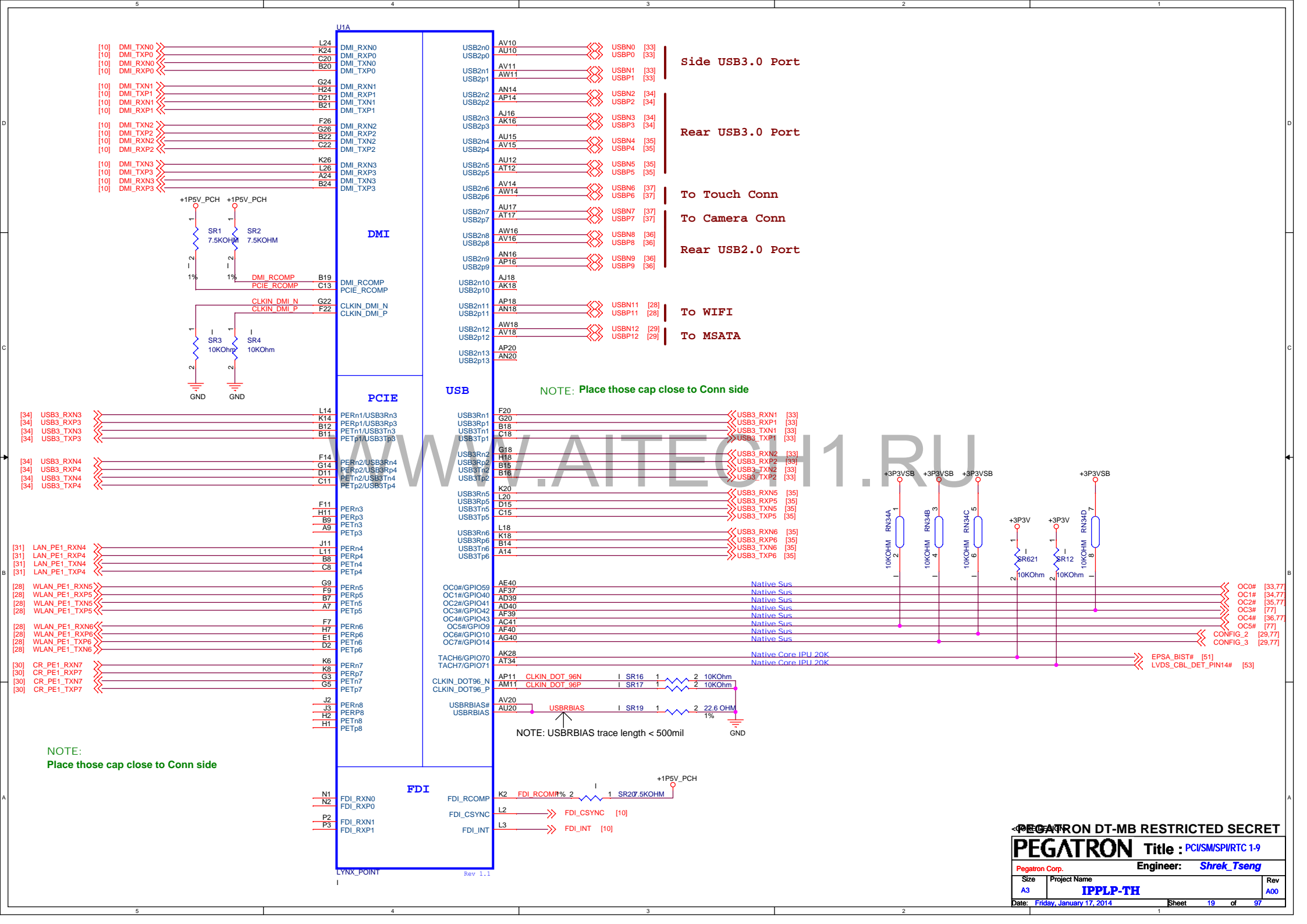
Size	Project Name	Rev
A3	IPPLP-TH	A00

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Place those cap inside CPU SOCKET cavity

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NOTE: CHASSIS ID

TYPE	ID2 GPIO 38	ID1 GPIO 17	ID0 GPIO 1
SFF	1	0	1
RESERVED	1	0	0
MT/DT	0	0	0
USFF	0	1	1
AIO	0	0	1
AIO UMA	0	1	0
AIO GPU	1	1	0

NOTE: Board ID Select

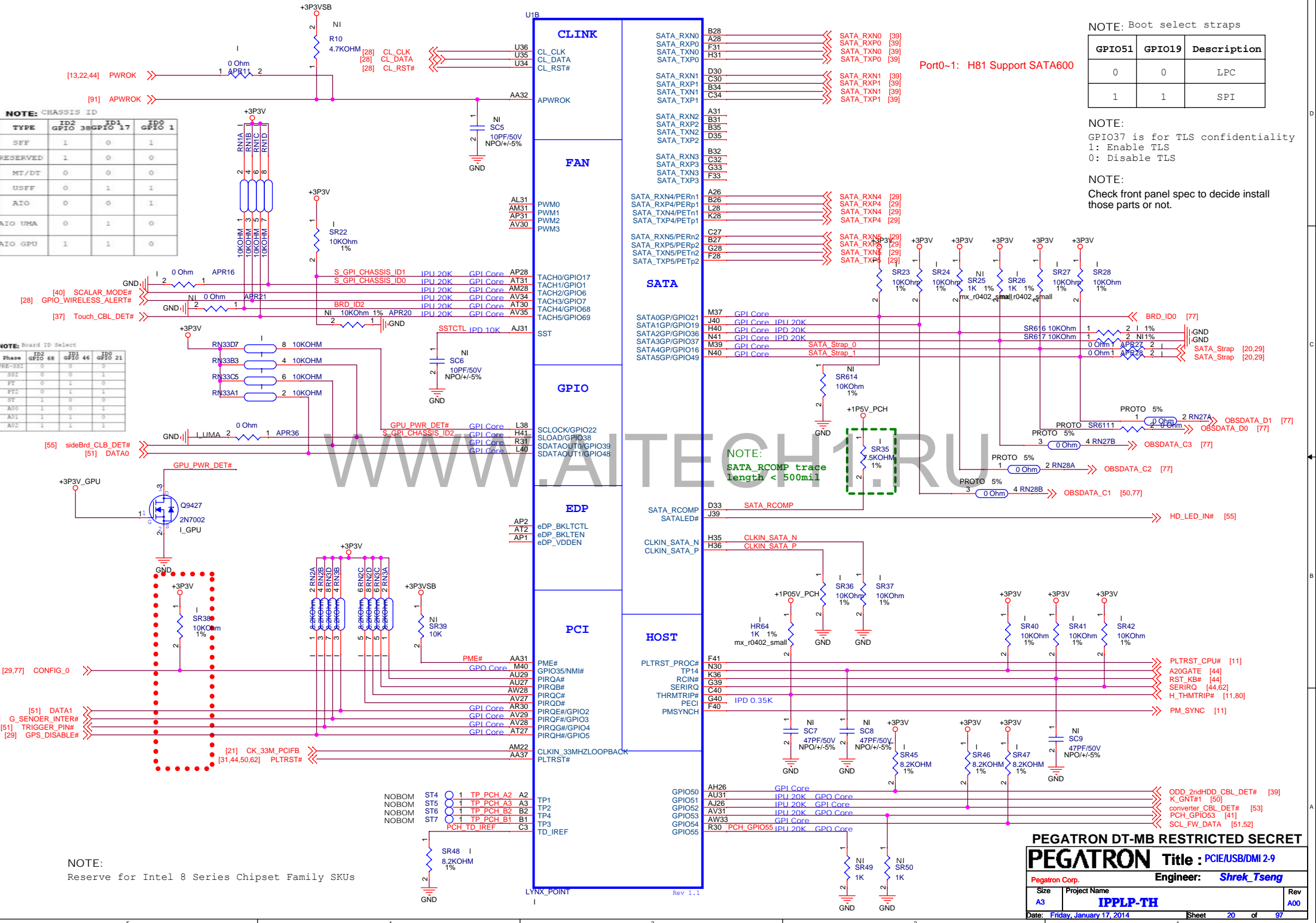
Phase	ID2 GPIO 66	ID1 GPIO 46	ID0 GPIO 21
PRE-POST	0	0	0
SS1	0	0	1
PF	0	1	0
PF2	0	1	1
BY	1	0	0
A00	1	0	1
A01	1	1	0
A02	1	1	1

NOTE: Boot select straps

GPIO51	GPIO19	Description
0	0	LPC
1	1	SPI

NOTE:
GPIO37 is for TLS confidentiality
1: Enable TLS
0: Disable TLS

NOTE:
Check front panel spec to decide install those parts or not.



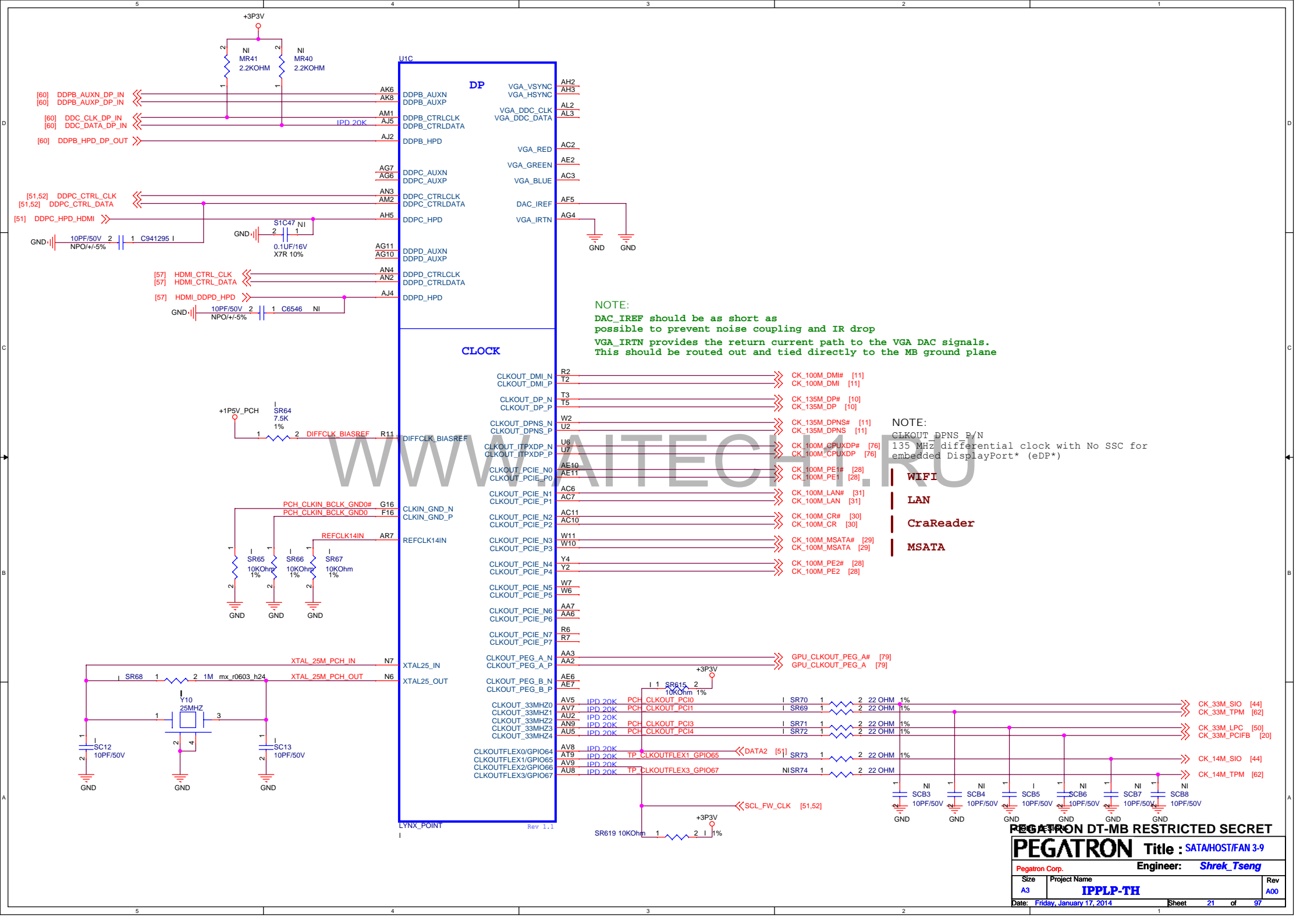
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIEUSB/DMI 2-9

Pegatron Corp. Engineer: Shrek_Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

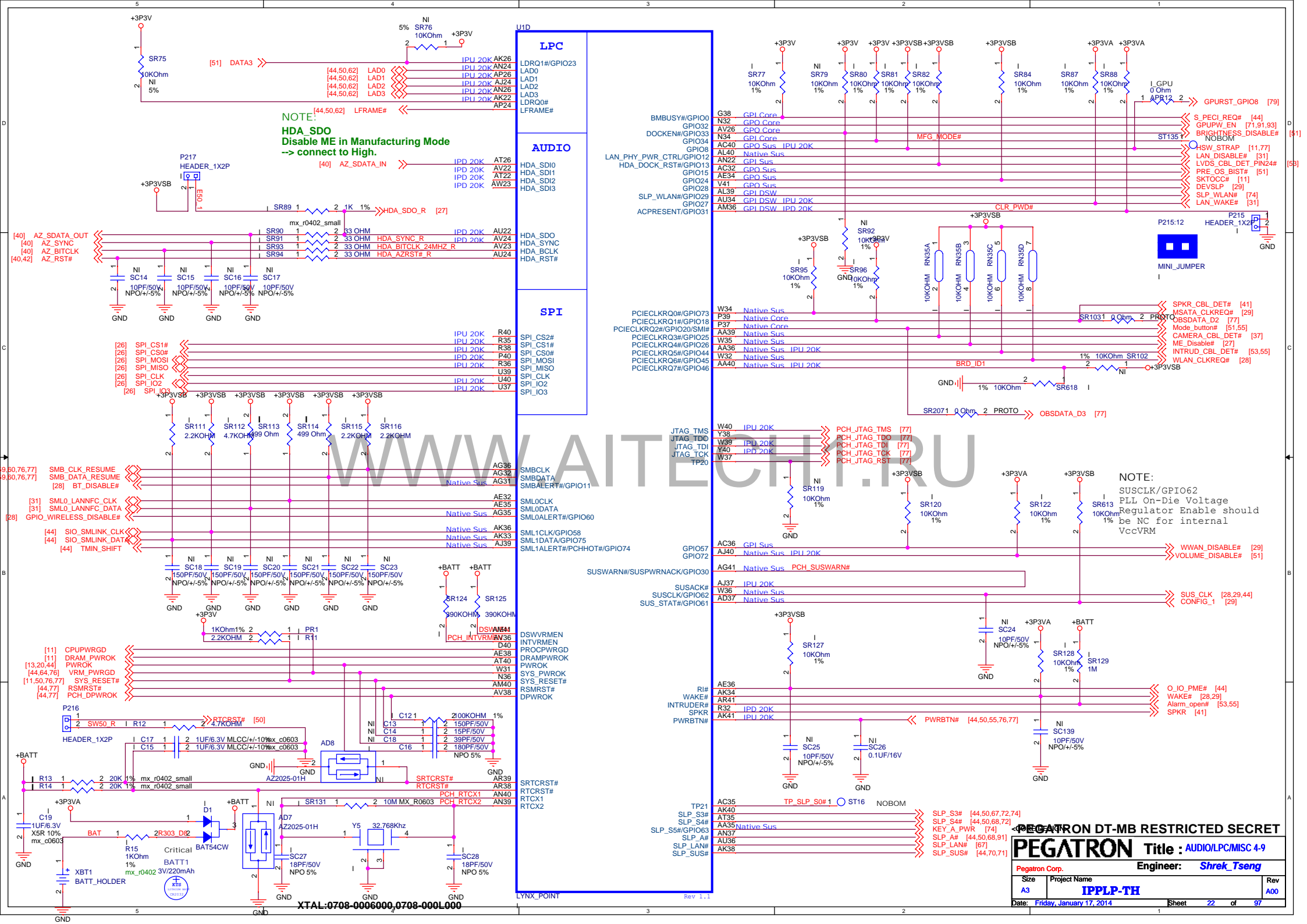
Date: Friday, January 17, 2014 Sheet 20 of 97



NOTE:
DAC_IREF should be as short as possible to prevent noise coupling and IR drop
VGA_IRTN provides the return current path to the VGA DAC signals.
This should be routed out and tied directly to the MB ground plane

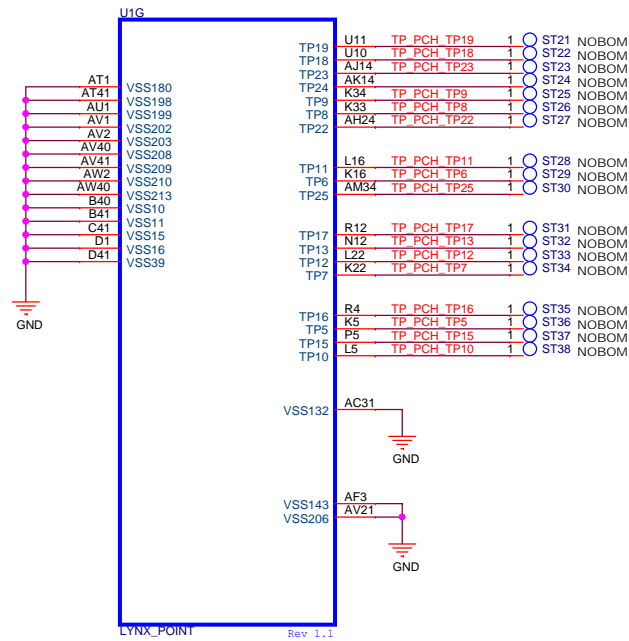
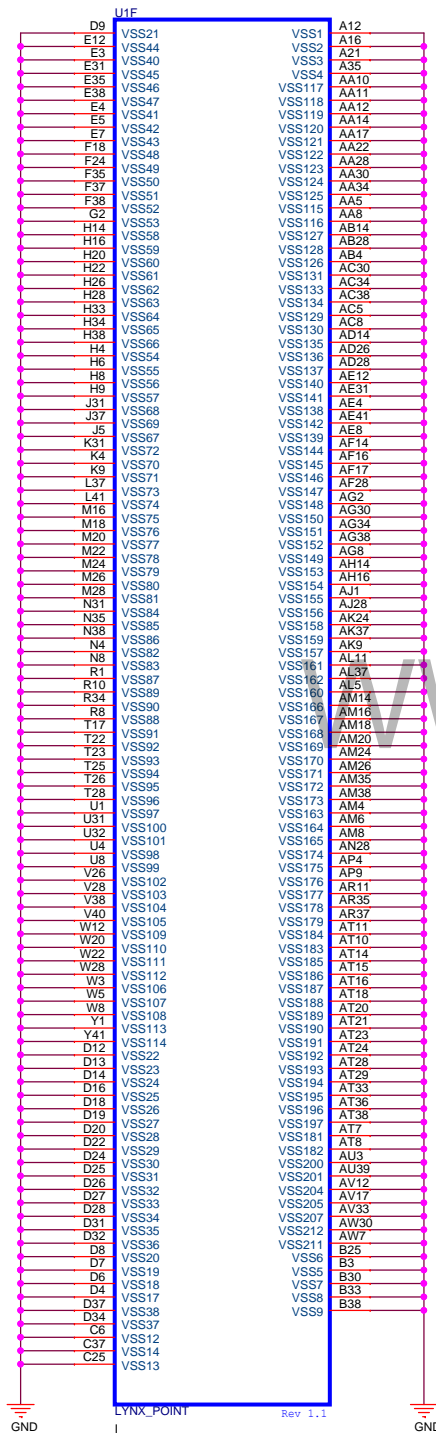
NOTE:
CLKOUT DPNS P/N
135 MHz differential clock with No SSC for embedded DisplayPort* (eDP*)

- WIFI
- LAN
- CraReader
- MSATA



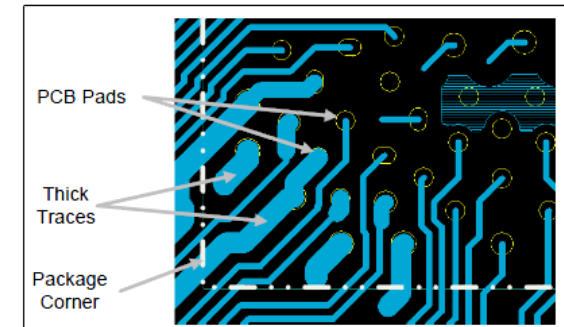
NOTE:
HDA_SDO
Disable ME in Manufacturing Mode
--> connect to High.

NOTE:
SUSCLK/GPIO62
PLL On-Die Voltage
Regulator Enable should
be NC for internal
VccVRM



Remove Heatsink

NOTE: Solder Pad Recommendation



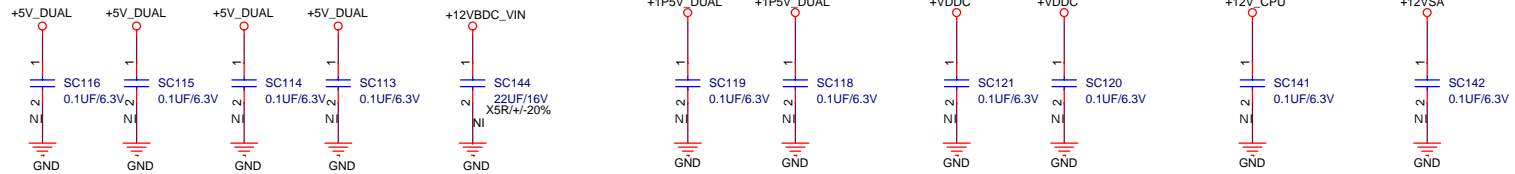
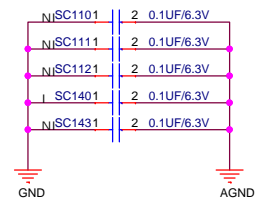
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CLK/NVRAM/FDI 6-9

Pegatron Corp. Engineer: Shrek Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

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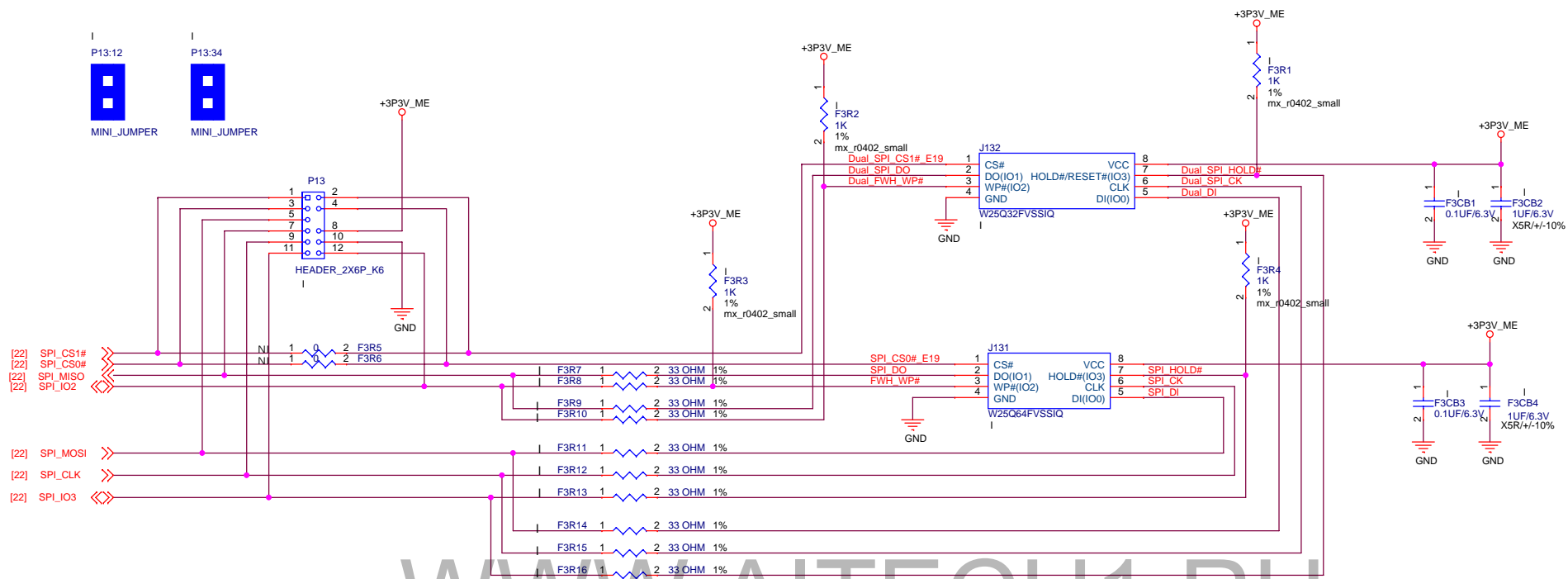
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_DPWROK & SLP_SUS

Pegatron Corp. Engineer: Shrek_Tseng

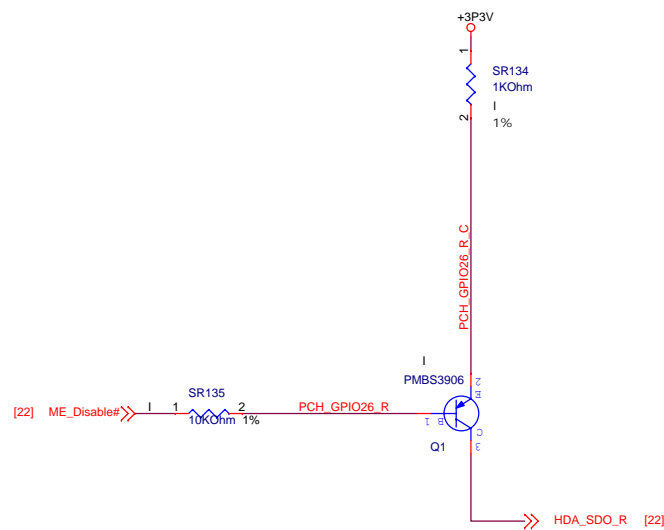
Size	Project Name	Rev
A3	IPPLP-TH	A00

Date: Friday, January 17, 2014 Sheet 25 of 97



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ME Disable



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PEGATRON DT-MB RESTRICTED SECRET

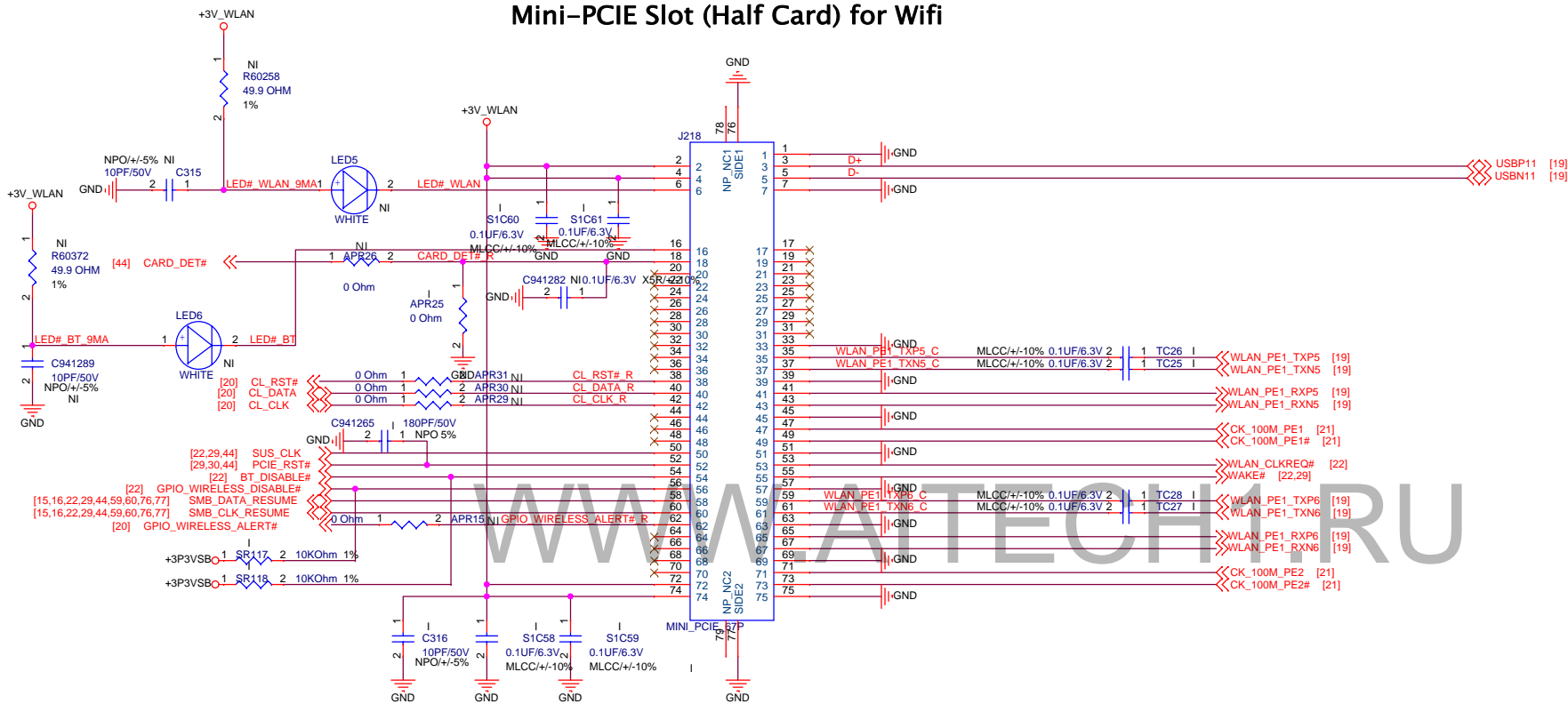
PEGATRON Title : ME DISABLE

Pegatron Corp. Engineer: Shrek_Tseng

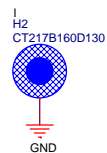
Size A3	Project Name IPPLP-TH	Rev A00
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Mini-PCIE Slot (Half Card) for Wifi



H=4mm



PEGATRON DT-MB RESTRICTED SECRET

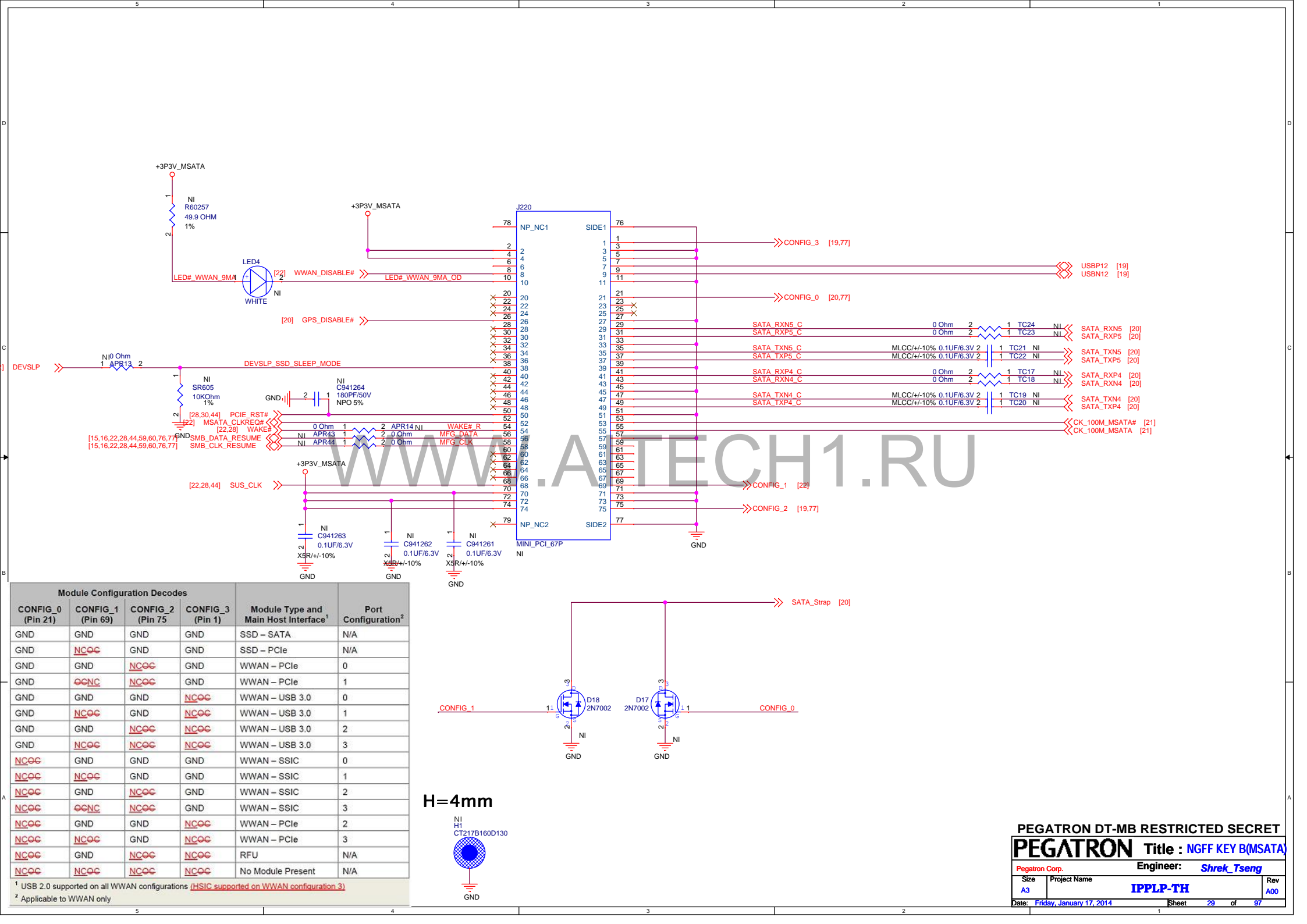
PEGATRON Title : NGFF KEY A(WLAN)

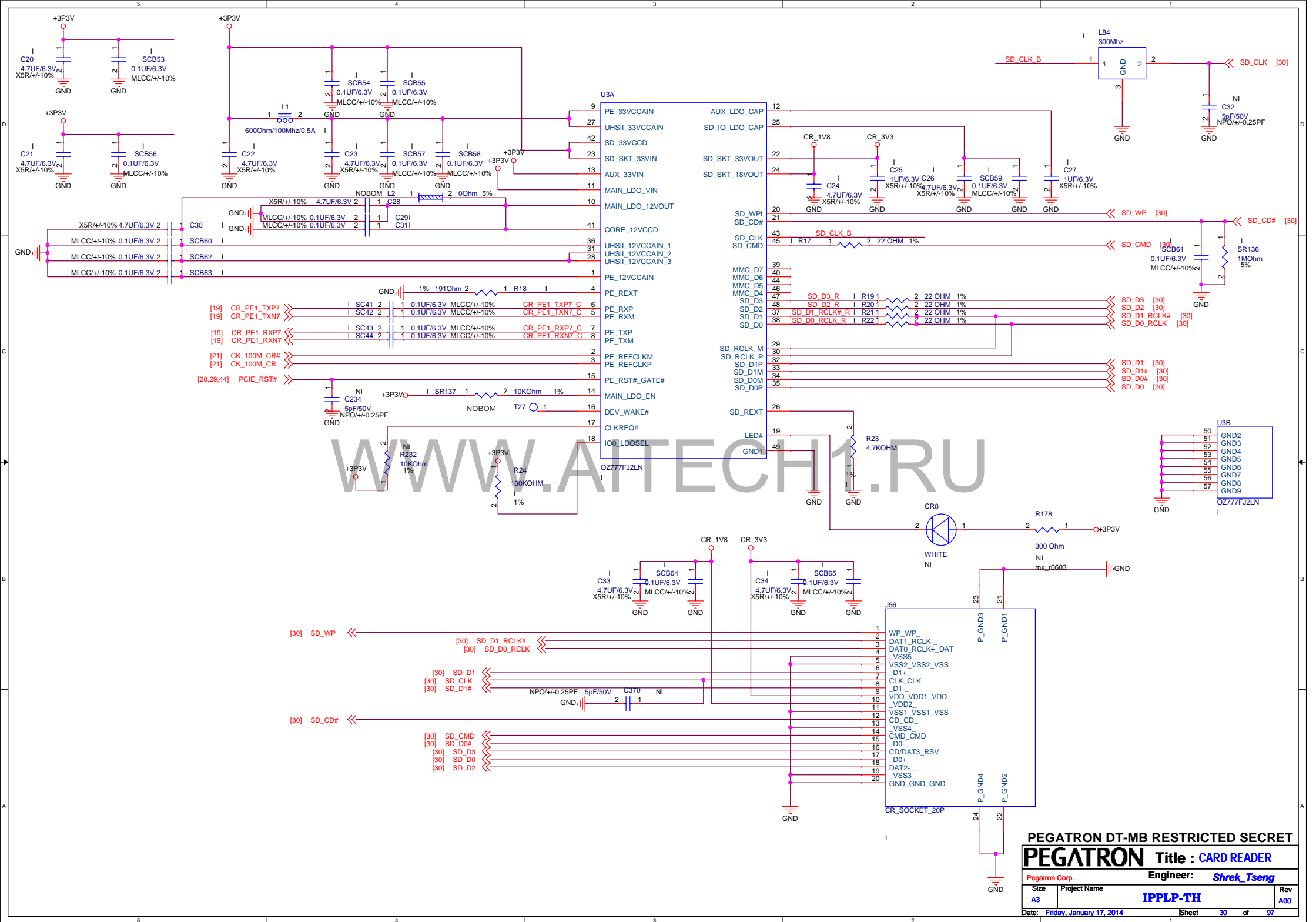
Pegatron Corp. Engineer: **Shrek_Tseng**

Size	Project Name	Rev
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A3	IPPLP-TH	A00
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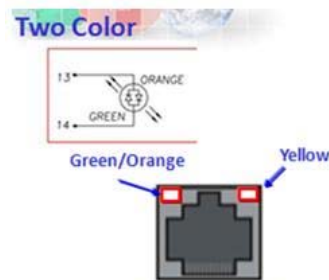
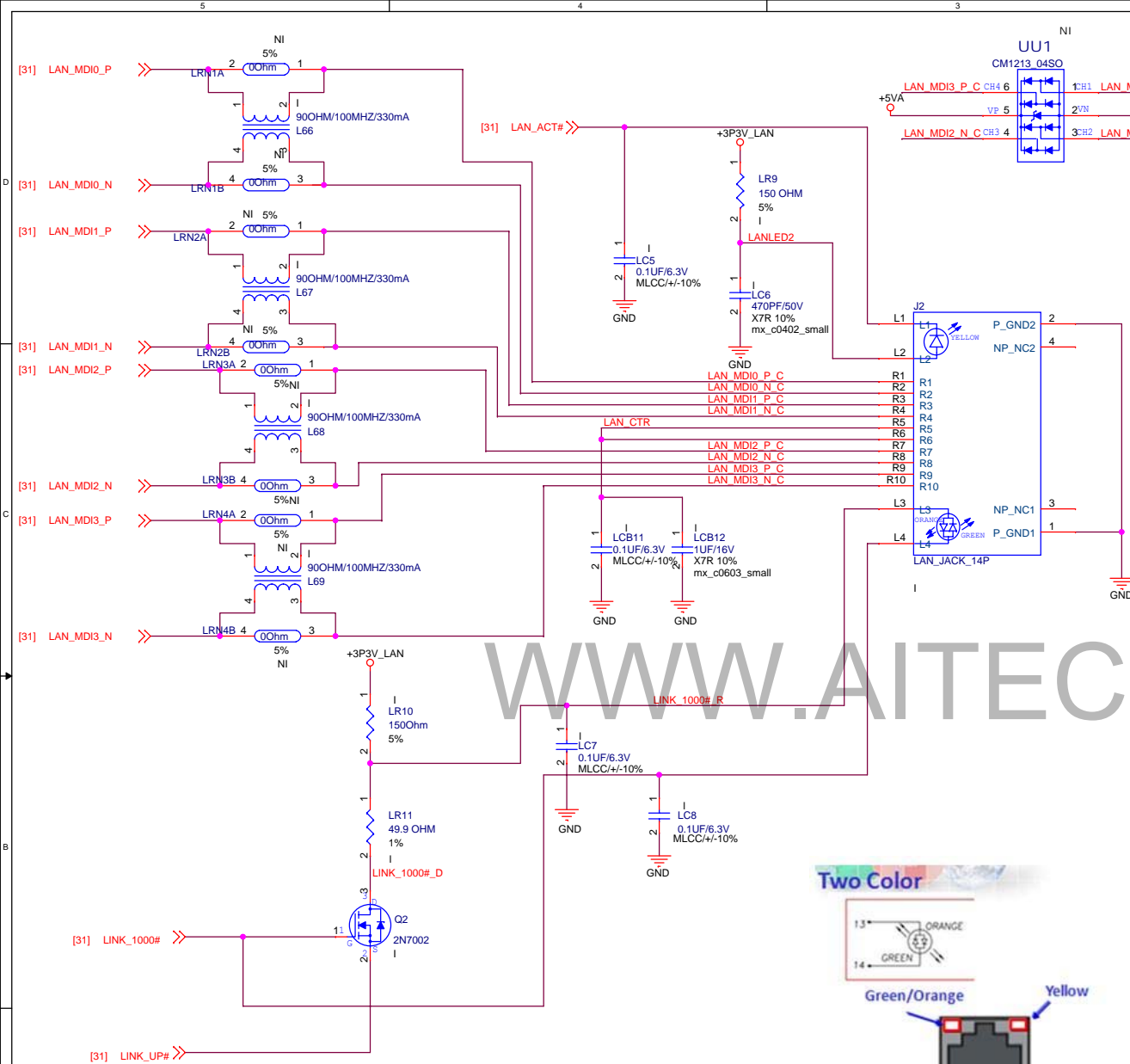
U4



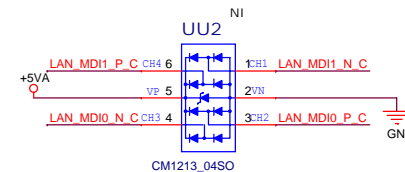
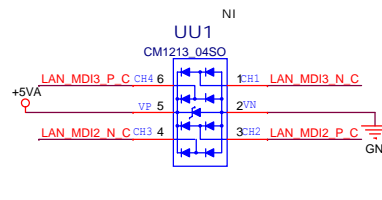
PEGATRON	Title : INTEL CLARKVILLE
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Size A3	Project Name IPPLP-TH	Rev A00
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Date: Friday, January 17, 2014 Sheet 31 of 97



Function	LINK LED State/Color	Active LED State/Color
No Link	OFF / NA	OFF / NA
Link 10Mbps	ON/Green	
Link 100Mbps	ON/Green	
Link 1000Mbps	ON/Orange	
No network activity		OFF / NA
Network activity		Blinking/Yellow



LED Modes Table

Mode	Selected Mode	Source Indication
000	Link 10/1000	Asserted when either 10 or 1000Mbps link is established and maintained
001	Link 100/1000	Asserted when either 100 or 1000Mbps link is established and maintained
010	Link Up	Asserted when any speed link is established and maintained.
011	Activity	Asserted when link is established and packets are being transmitted or received
100	Link/Activity	Asserted when link is established AND when there is NO transmit or receive activity
101	Link 10	Asserted when a 10Mbps link is established and maintained.
110	Link 100	Asserted when a 100Mbps link is established and maintained
111	Link 1000	Asserted when a 1000Mbps link is established and maintained

LED Configuration PHY Address 01, Page 0, Register 30

Name	Default	Bits	Description	Type
Blink rate	0b	15	Specifies the blink mode of the LEDs. 0b = Blinks at 200 ms on and 200 ms off. 1b = Blinks at 83 ms on and 83 ms off.	RW
LED2 Blink	0b	14	LED2_BLINK Field 0b = No blinking. 1b = Blinking.	RW
LED2 Invert	0b	13	LED2_IVRT Field 0b = Active low output. 1b = Active high output.	RW

LED Configuration PHY Address 01, Page 0, Register 30

Name	Default	Bits	Description	Type
LED2 Mode	110b	12:10	Mode specifying what event/state/pattern is displayed on LED2.	RW
LED1 Blink	0b	9	LED1_BLINK Field 0b = No blinking. 1b = Blinking.	RW
LED1 Invert	0b	8	LED1_IVRT Field 0b = Active low output. 1b = Active high output.	RW
LED1 Mode	111b	7:5	Mode specifying what event/state/pattern is displayed on LED1.	RW
LED0 Blink	1b	4	LED0_BLINK Field 0b = No blinking. 1b = Blinking.	RW
LED0 Invert	0b	3	LED0_IVRT Field 0b = Active low output. 1b = Active high output.	RW
LED0 Mode	100b	2:0	Mode specifying what event/state/pattern is displayed on LED0.	RW

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LAN JACK

Pegatron Corp. Engineer: Shrek_Tseng

Size A3 Project Name IPPLP-TH

Date: Friday, January 17, 2014 Sheet 32 of 97

1213-00LN000 USB2.0

PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	PGND
REMARK	USB2.0 CONTACT PIN			

NOTE:

0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB

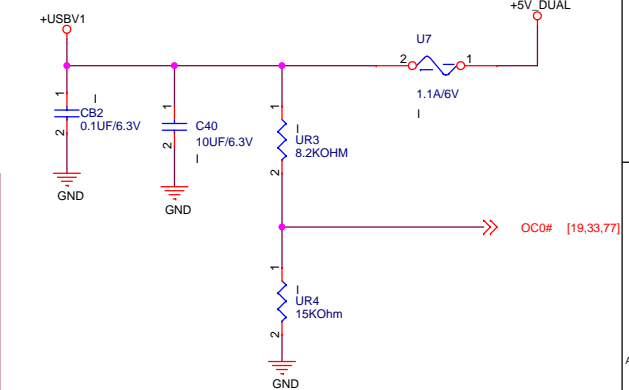
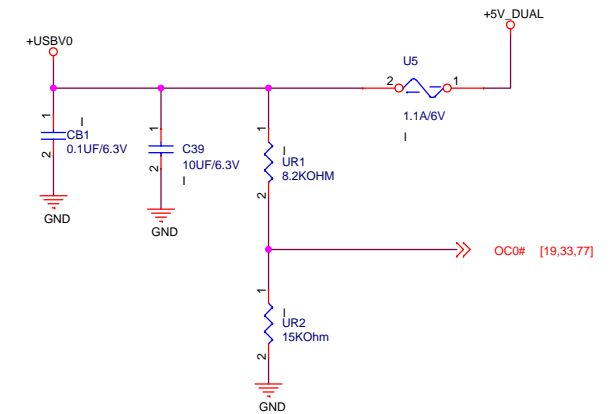
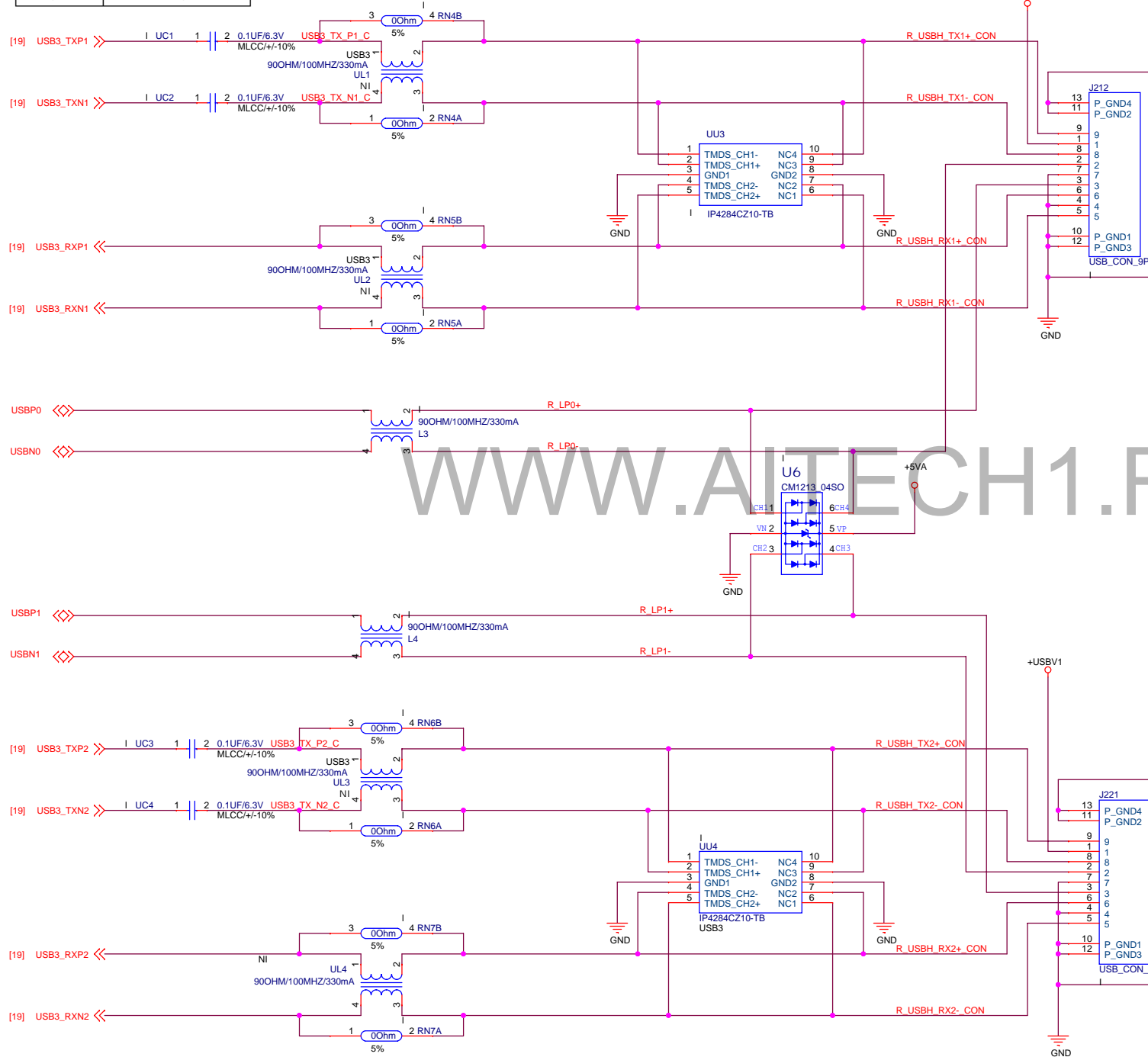
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI

Gold flash only

Co-lay USB connector

1213-00LH000 USB3.0

1213-00LN000 USB2.0



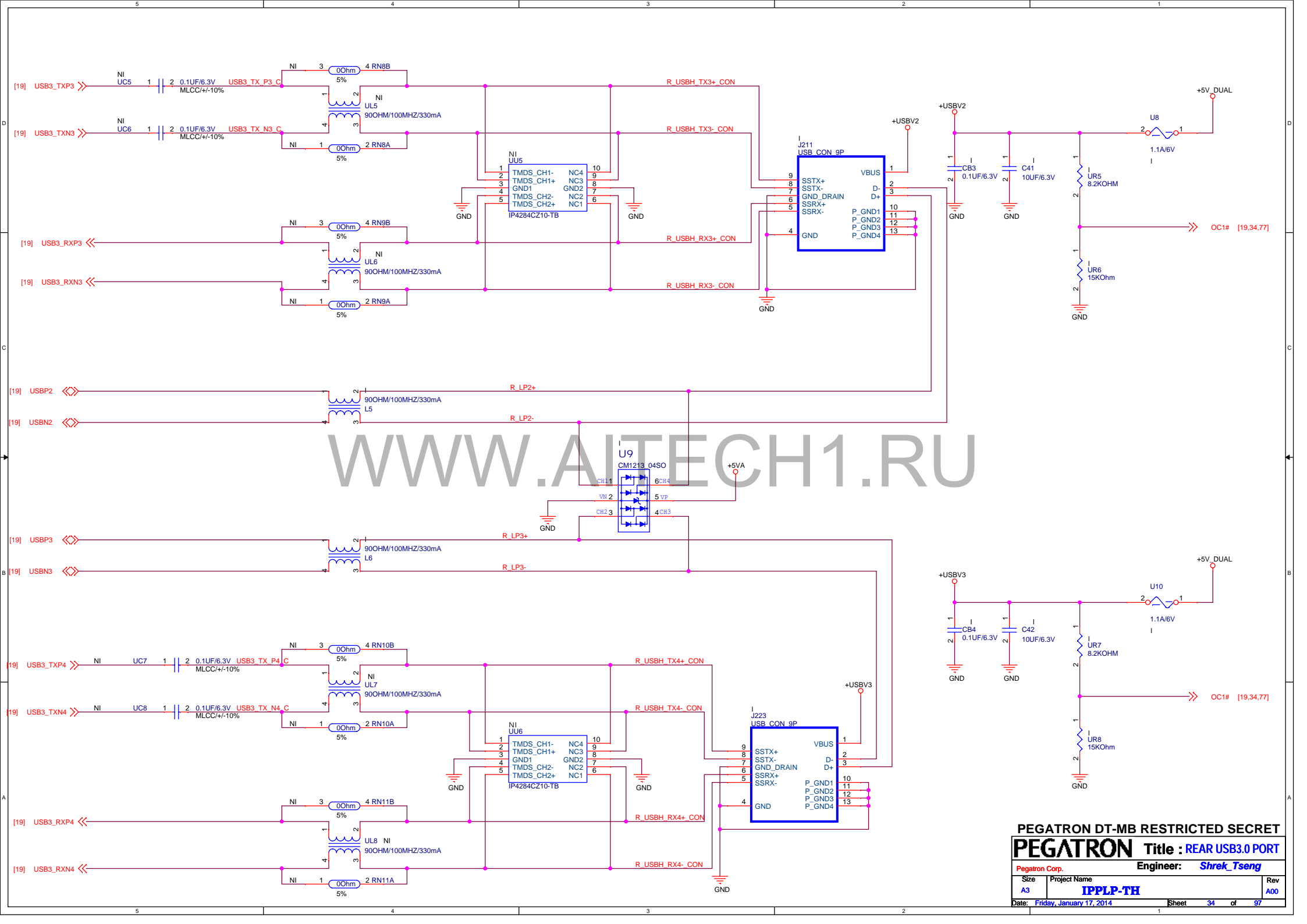
PEGATRON DT-MB RESTRICTED SECRET

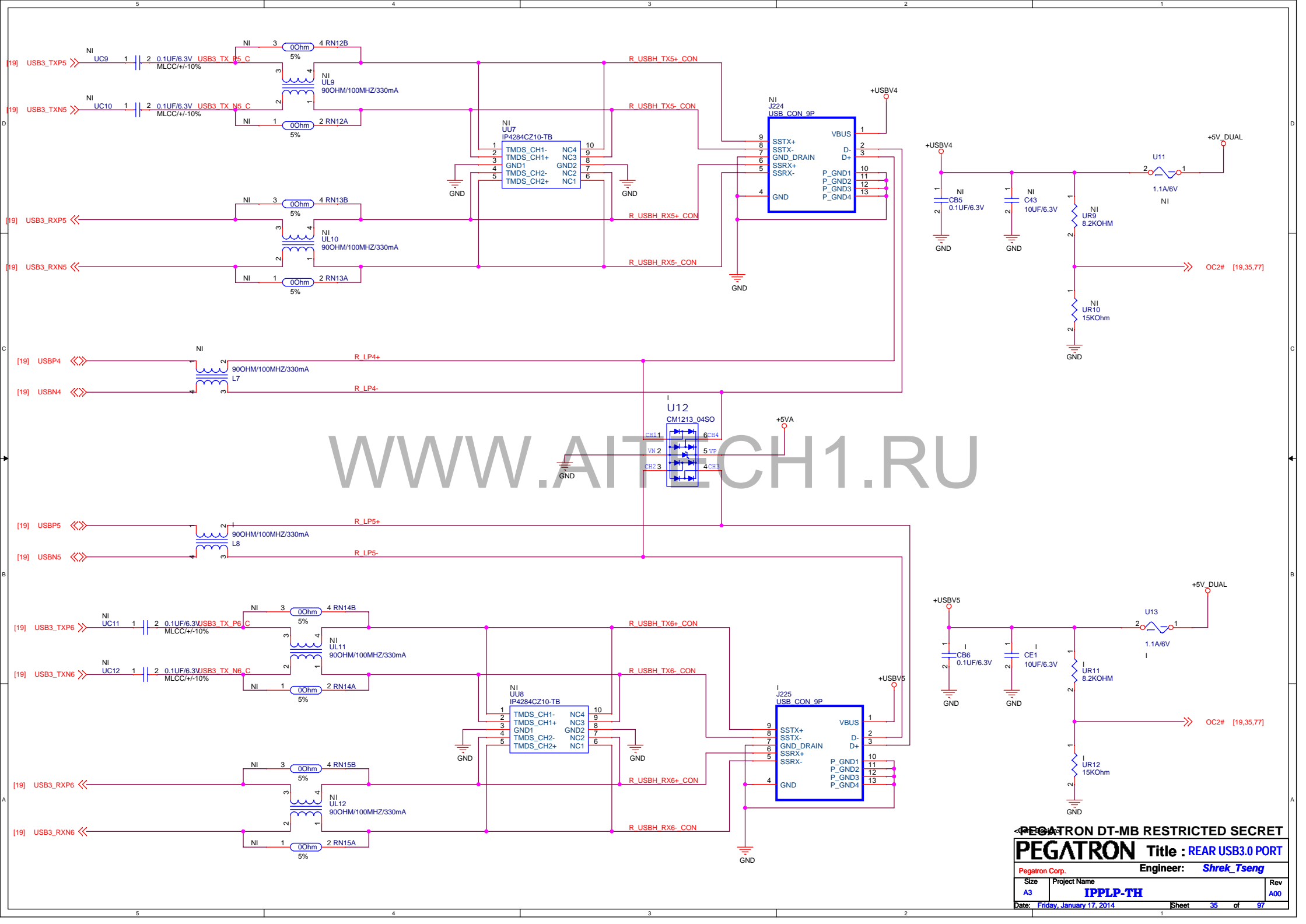
PEGATRON Title : SIDE USB3.0 PORT

Pegatron Corp. Engineer: Shrek_Tseng

Size A3 Project Name IPPLP-TH Rev A00

Date: Friday, January 17, 2014 Sheet 33 of 97





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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **XXXXXX**

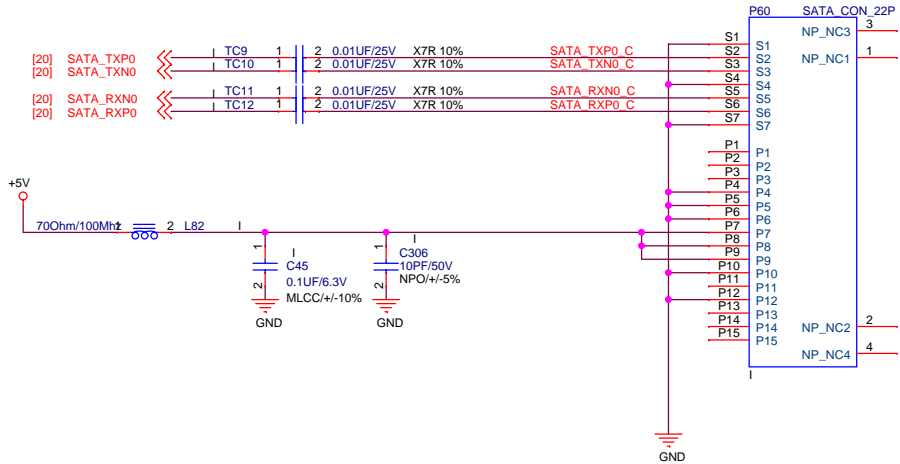
Pegatron Corp. Engineer: **Shrek Tseng**

Size A3	Project Name IPPLP-TH	Rev A00
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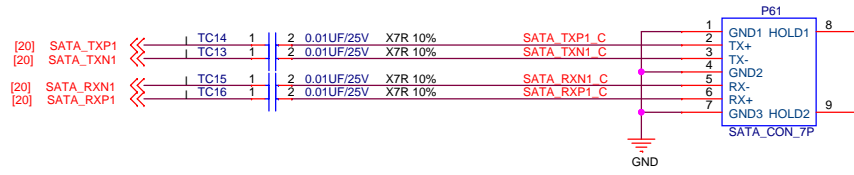
Date: **Friday, January 17, 2014** Sheet **38** of **97**

SATA CONNECTOR

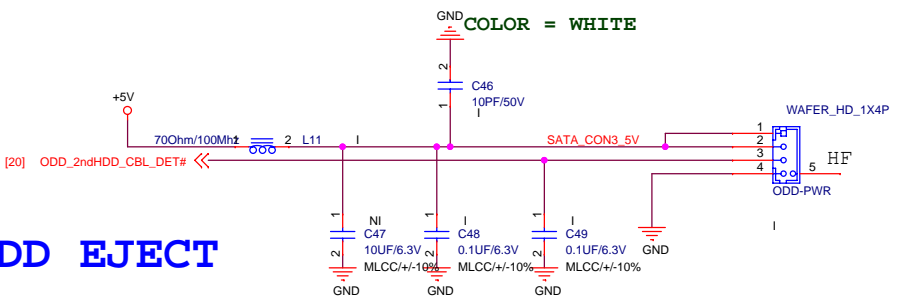
NOTE:
Place those Cap close to Conn sode
To Conn distance are less then 500mils



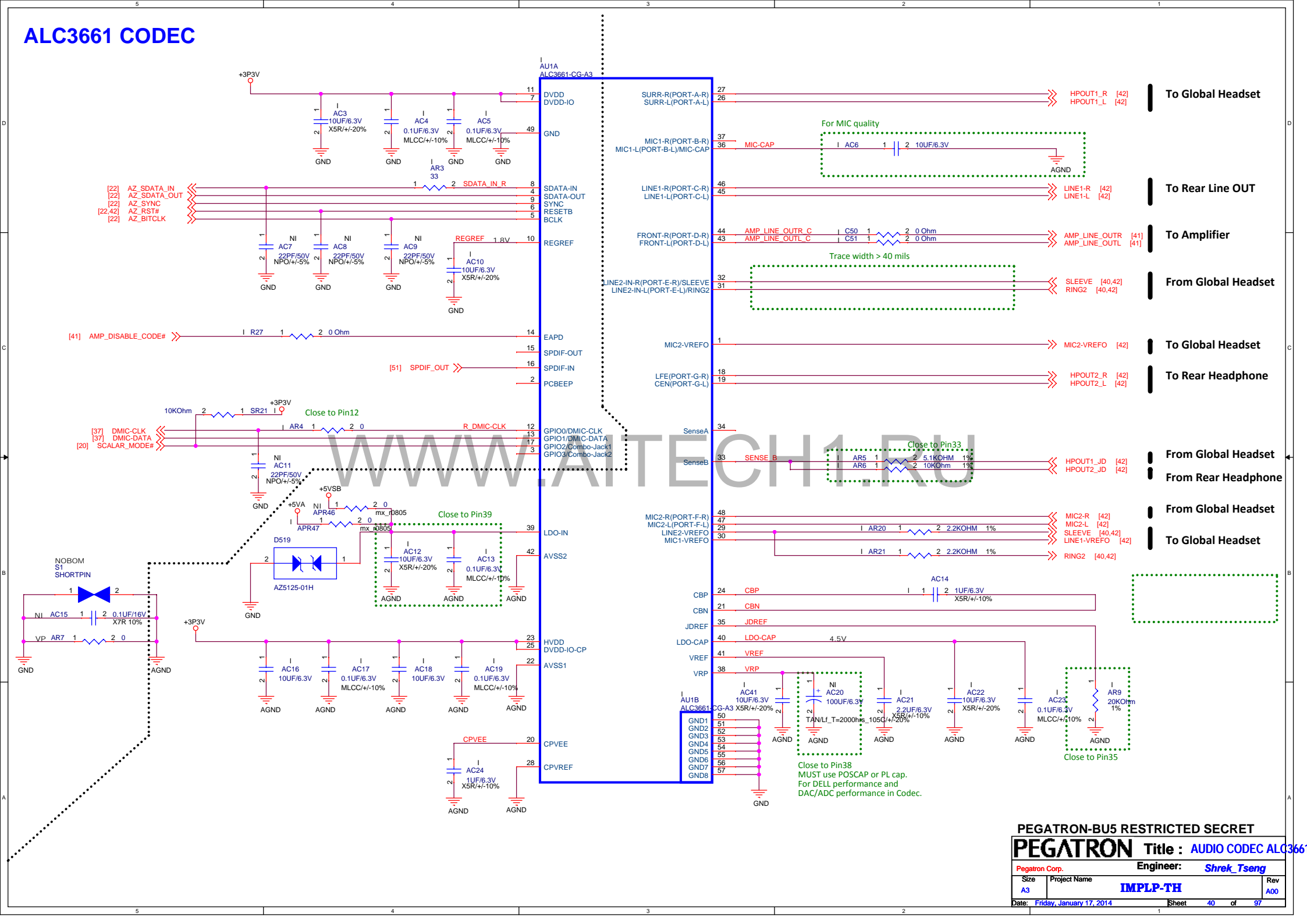
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ODD EJECT



ALC3661 CODEC



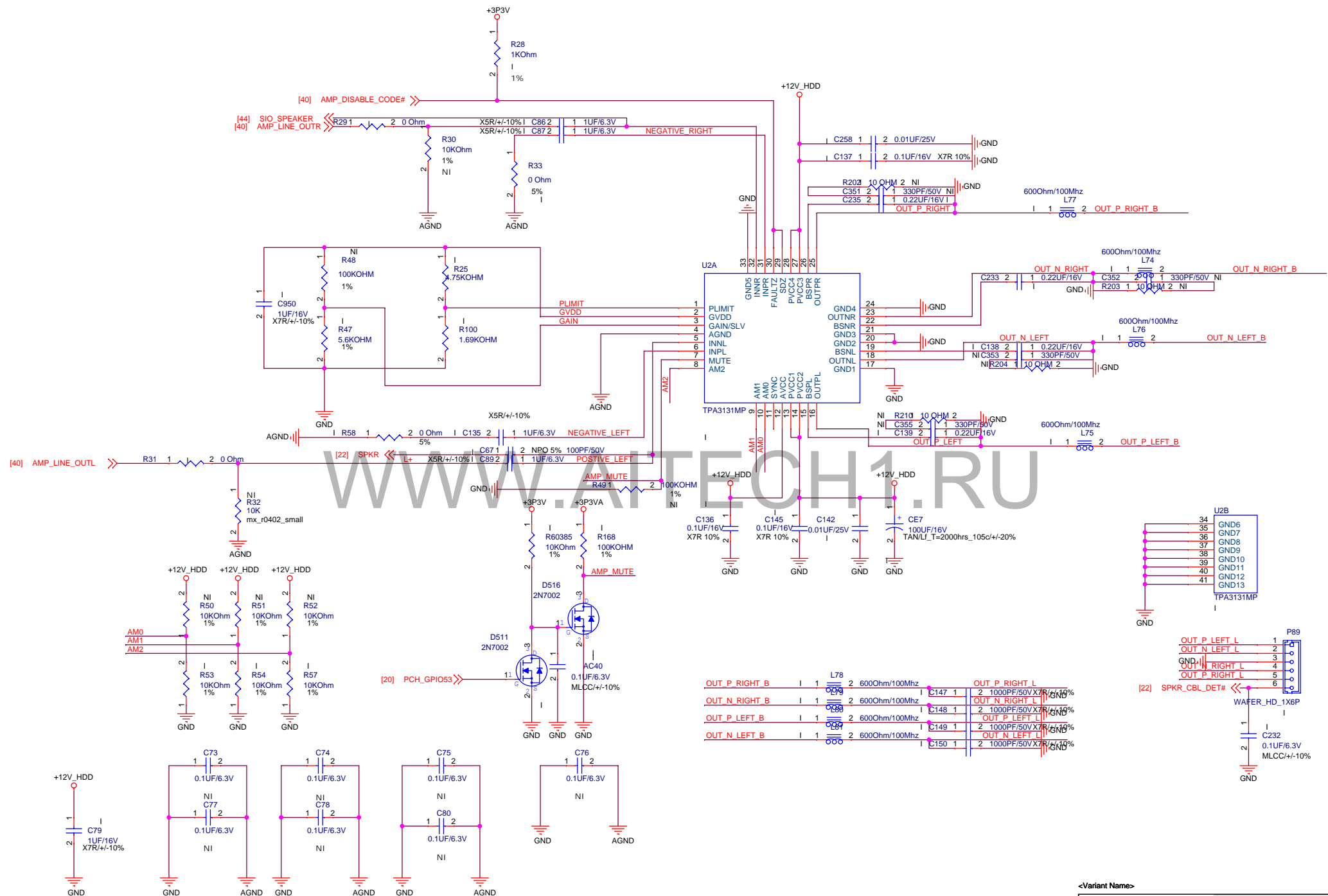
PEGATRON-BU5 RESTRICTED SECRET

PEGATRON Title : AUDIO CODEC ALC3661

Pegatron Corp. Engineer: Shrek Tseng

Size A3 Project Name IMPLP-TH Rev A00

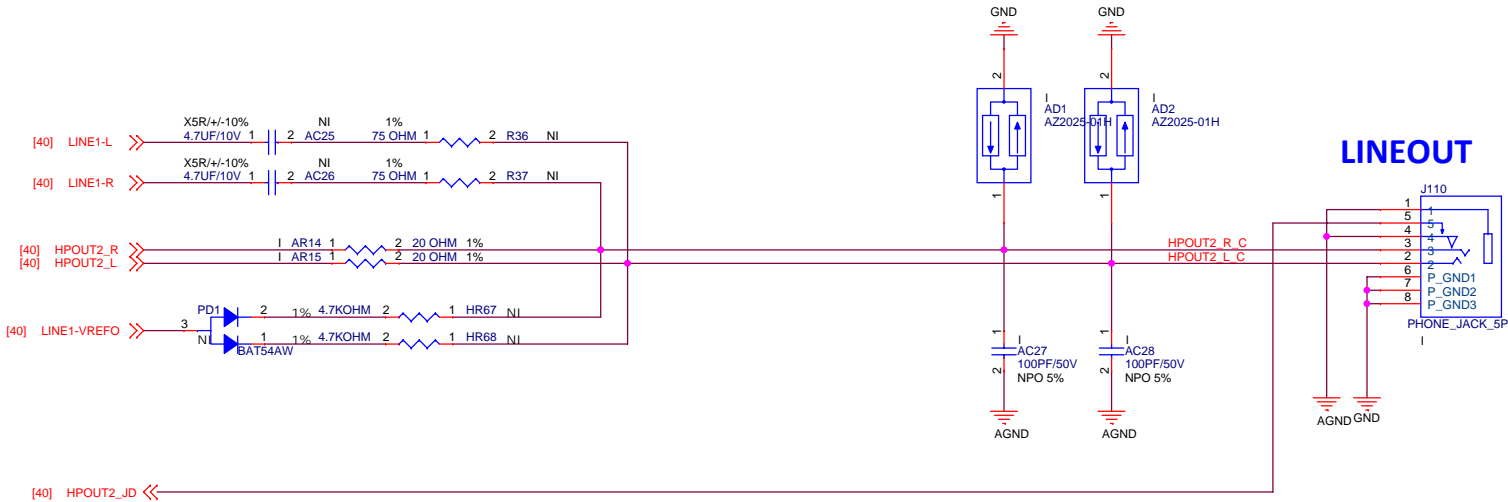
Date: Friday, January 17, 2014 Sheet 40 of 97



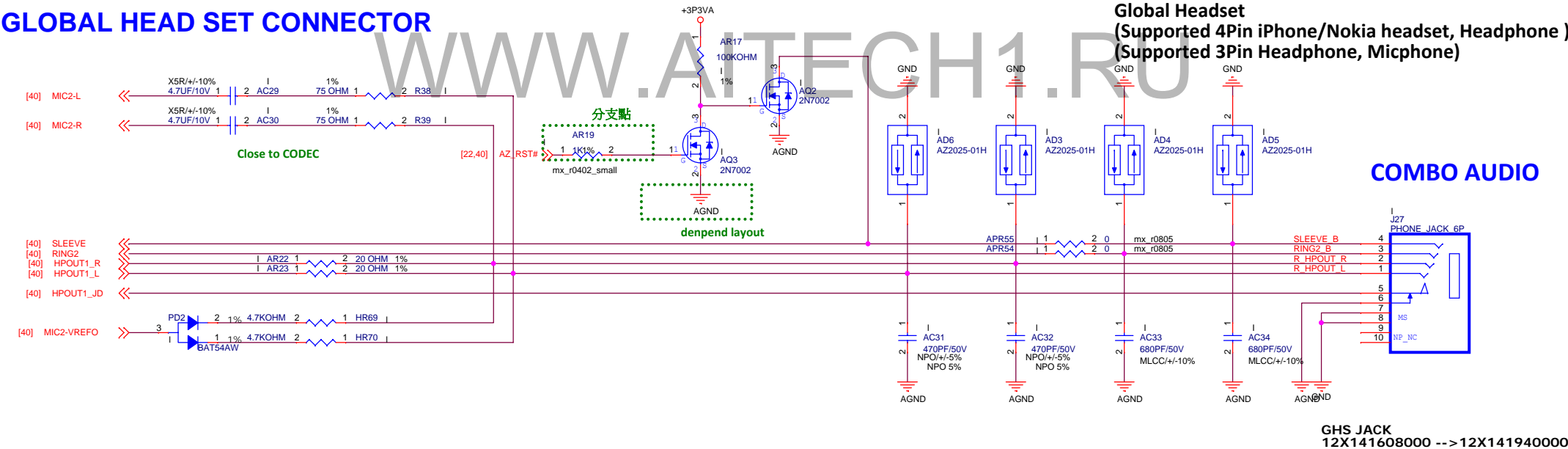
<Variant Name>

PEGATRON		Title : AMP	
Pegatron Corp.		Engineer: <i>Shrek_Tseng</i>	
Size A3	Project Name IPPLP-TH	Rev A00	
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REAR LINE-OUT
Support Re-Tasking Function



GLOBAL HEAD SET CONNECTOR



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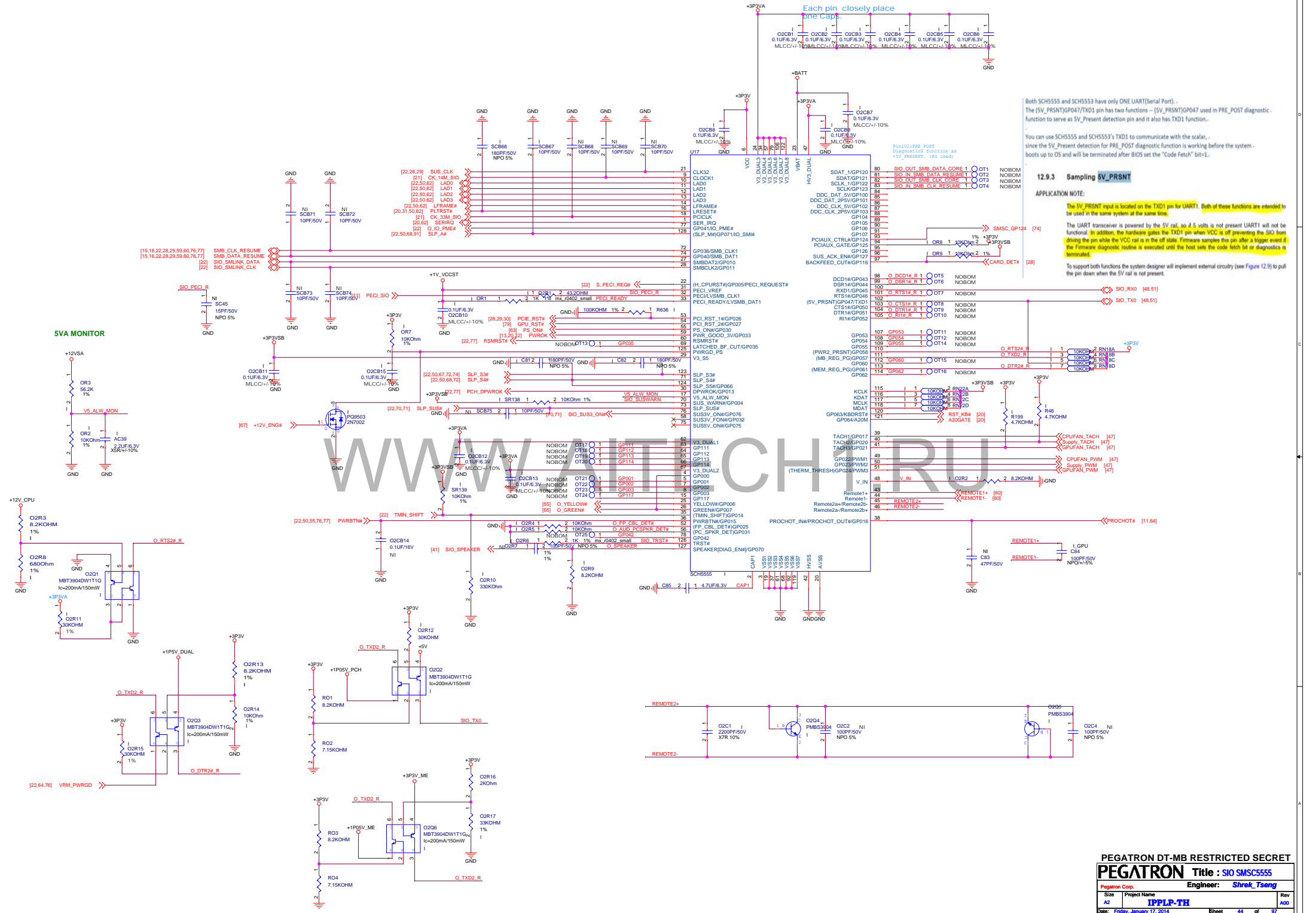
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : XXXXXX

Pegatron Corp. Engineer: Shrek_Tseng

Size A3	Project Name IPPLP-TH	Rev A00
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Both SCH5555 and SCH5553 have only ONE UART(Serial Port).
The (SV_PRESNT)GP047/TXD1 pin has two functions -- (SV_PRESNT)GP047 used in PRE_POST diagnostic function to serve as SV_Present detection pin and it also has TXD1 function.
You can use SCH5555 and SCH5553's TXD1 to communicate with the scalar,
since the SV_Present detection for PRE_POST diagnostic function is working before the system boots up to OS and will be terminated after BIOS set the "Code Fetch" bit=1.

12.9.3 Sampling SV_PRESNT

APPLICATION NOTE:
The SV_PRESNT input is located on the TXD1 pin for UART1. Both of these functions are intended to be used in the same system at the same time.

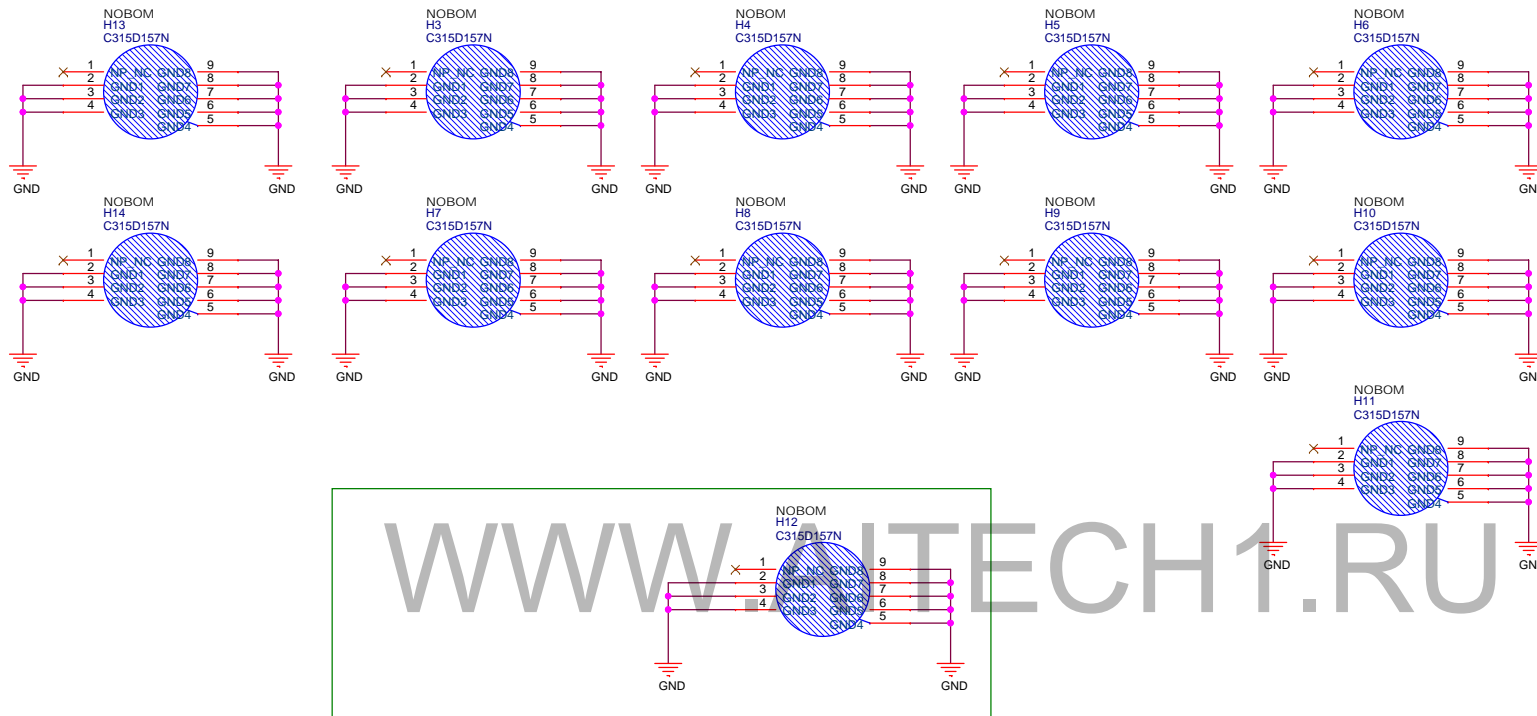
The UART transceiver is powered by the 5V rail, so if 5 volts is not present UART1 will not be functional. In addition, the hardware gates the TXD1 pin when VCC is off preventing the SIO from driving the pin while the VCC rail is in the off state. Firmware samples this pin after a trigger event if the Firmware diagnostic routine is executed until the host sets the code fetch bit or diagnostics is terminated.

To support both functions the system designer will implement external circuitry (see Figure 12.9) to pull the pin down when the SV rail is not present.

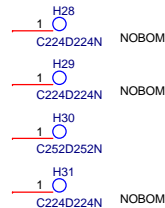
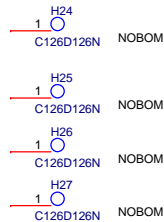
WWW.AITECH1.RU

PEGATRON DT-MB RESTRICTED SECRET

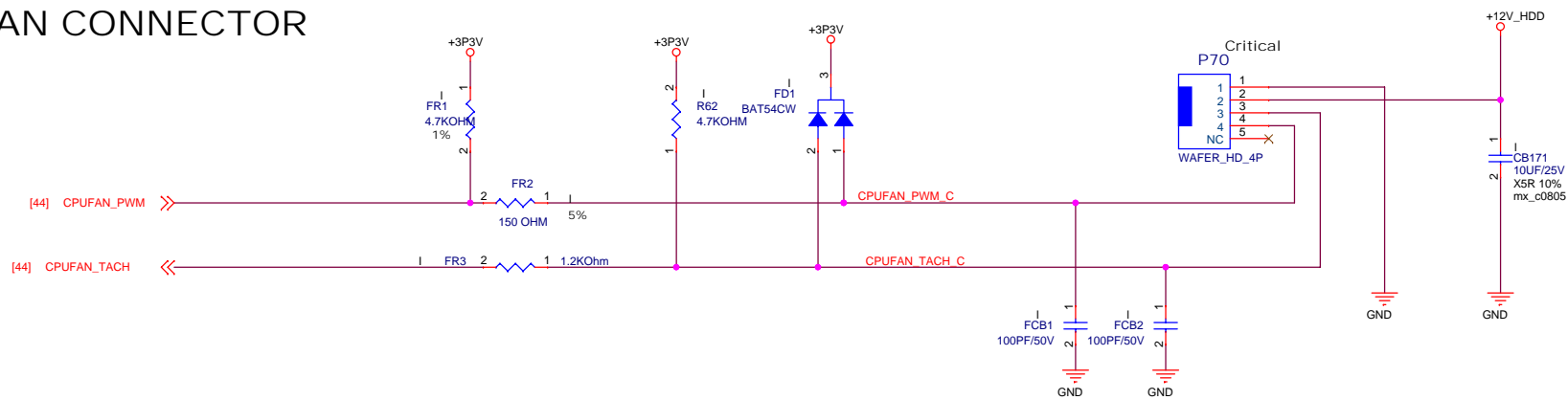
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Pegatron Corp.		Engineer: Shrek Tseng	
Size	Project Name	Rev	
A3	IPPLP-TH	A00	
Date: Friday, January 17, 2014		Sheet	45 of 97



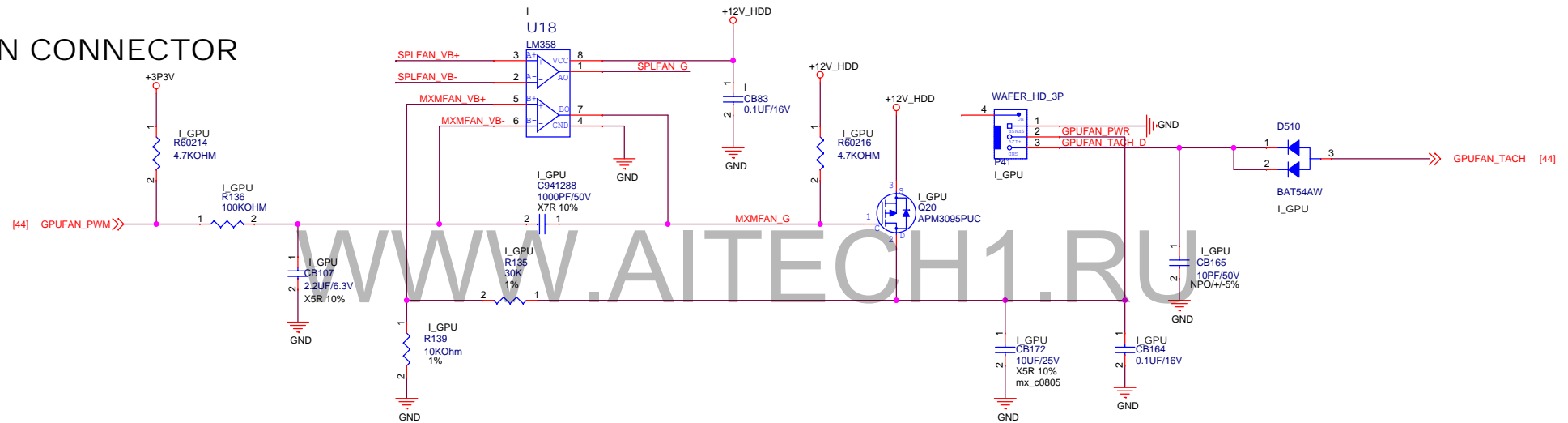
GPU SHOLE



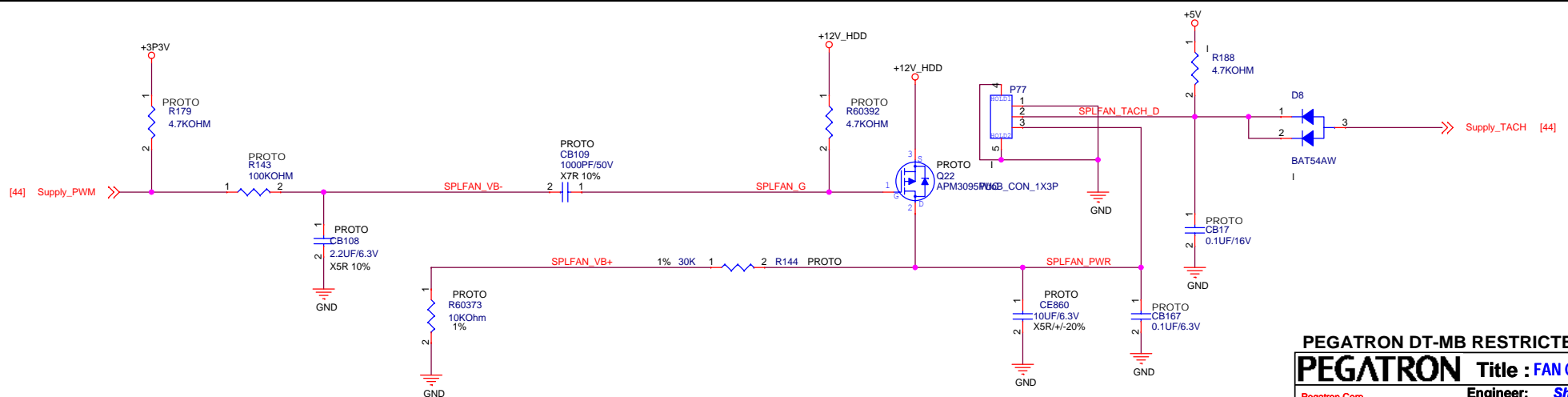
GPU FAN CONNECTOR



GPU FAN CONNECTOR



POWER SUPPLY FAN CONNECTOR



PEGATRON Title : **FAN CIRCUIT**

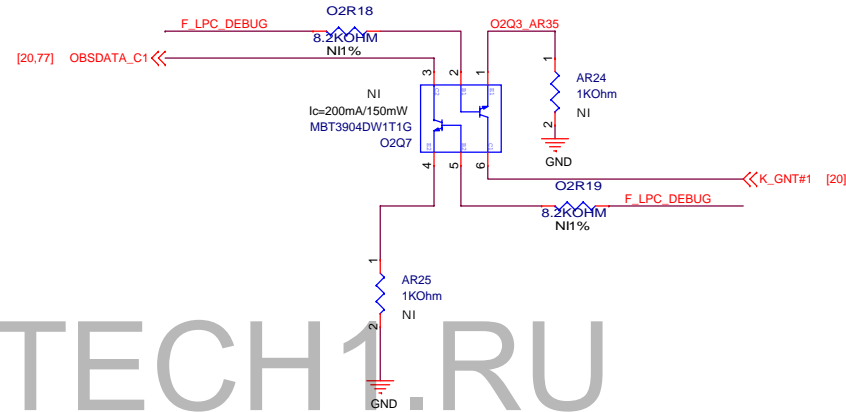
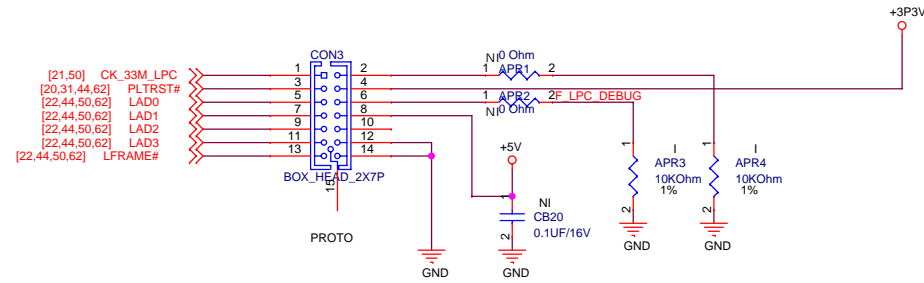
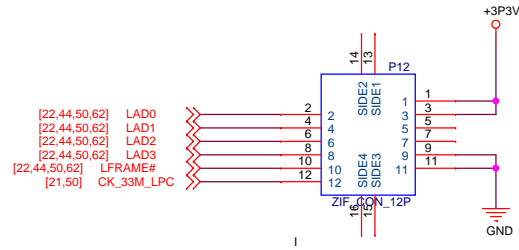
Size A3	Project Name IPPLP-TH	Rev A00
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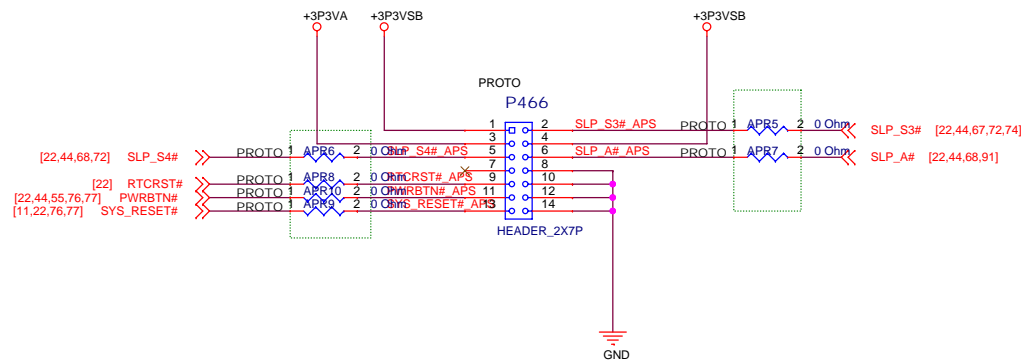
WWW.AITECH1.RU

Debug Card CON



WWW.AITECH1.RU

APS



PEGATRON DT-MB RESTRICTED SECRET

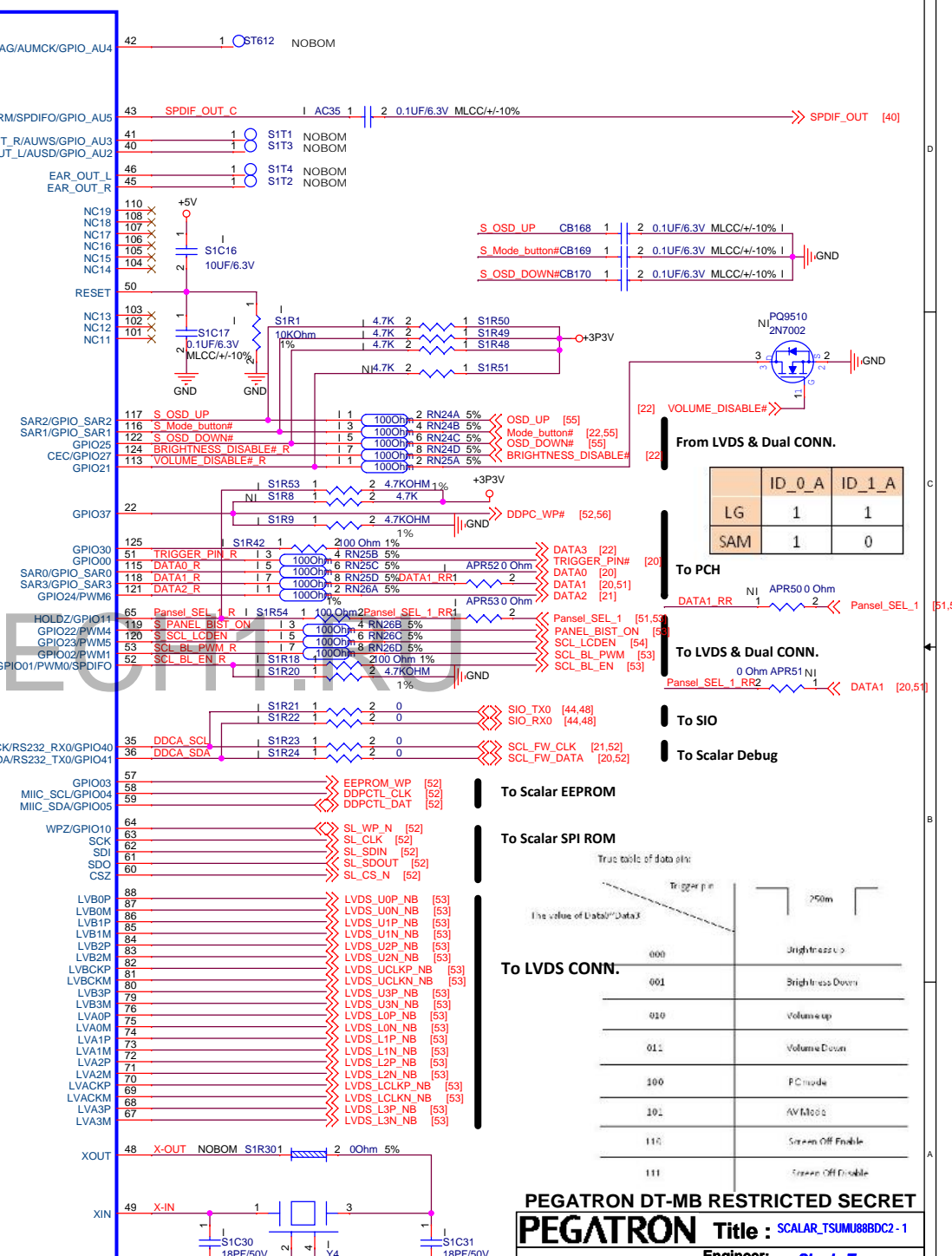
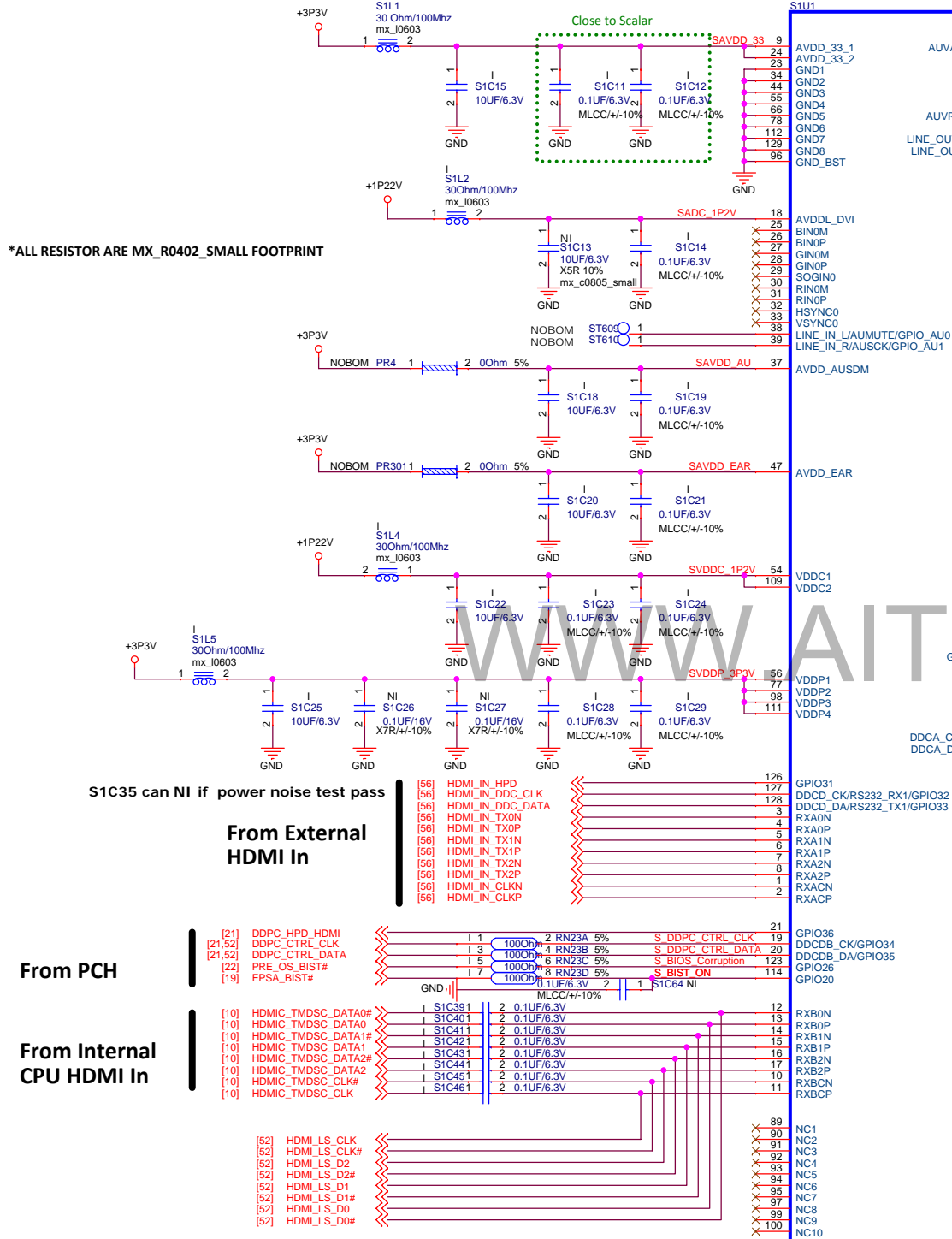
PEGATRON Title : APS/LPC DEBUG

Pegatron Corp. Engineer: Shrek Tseng

Size A3 Project Name IPPLP-TH Rev A00

Date: Friday, January 17, 2014 Sheet 50 of 97

*ALL RESISTOR ARE MX_R0402_SMALL FOOTPRINT



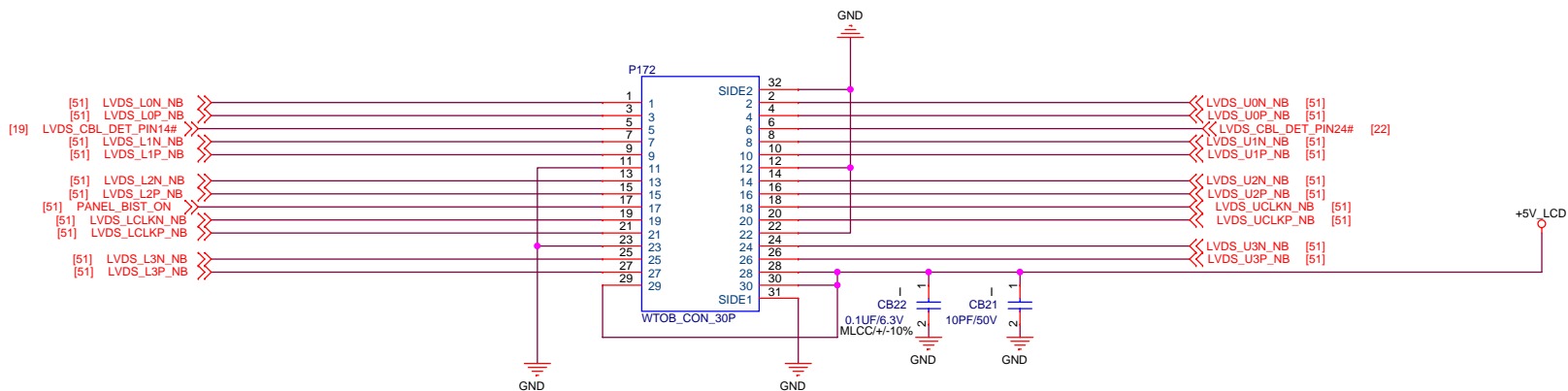
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SCALAR_TSUMU88BC2-1

Pegatron Corp. Engineer: Shrek Tseng

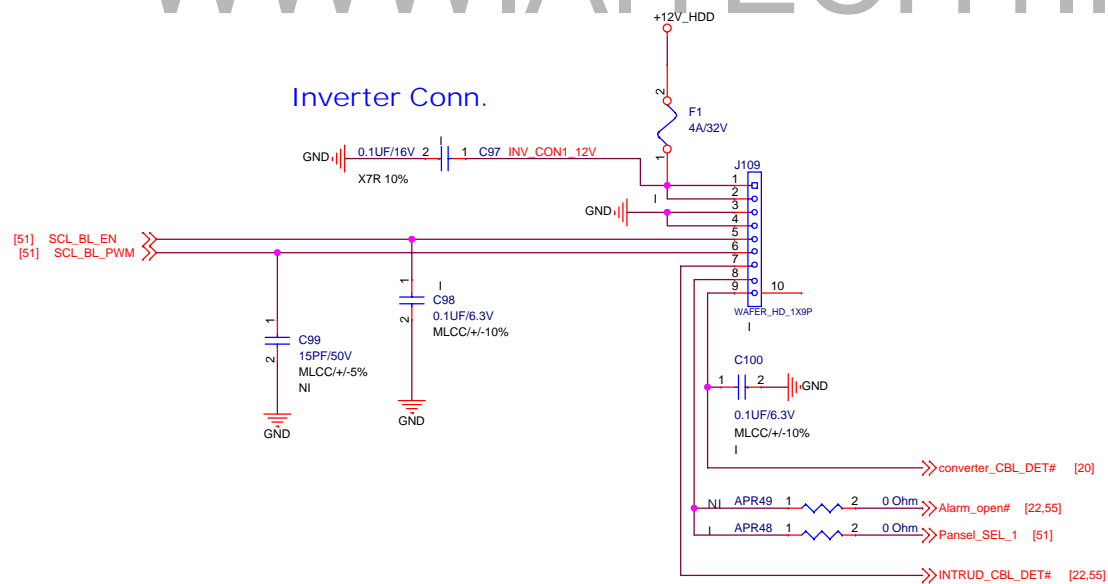
Size A3 Project Name IPPLP-TH Rev A00

Date: Friday, January 17, 2014 Sheet 51 of 97



CONVERTER CONN.

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LVDS & CONVERTER C

Pegatron Corp. Engineer: Shrek Tseng

Size	Project Name	Rev
A3	IPPLP-TH	A00

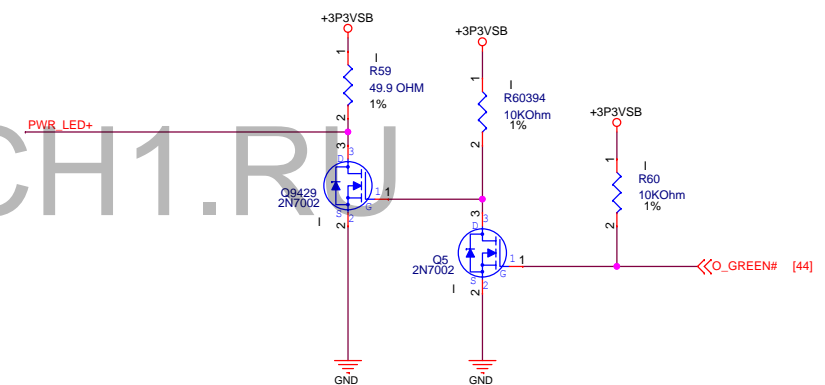
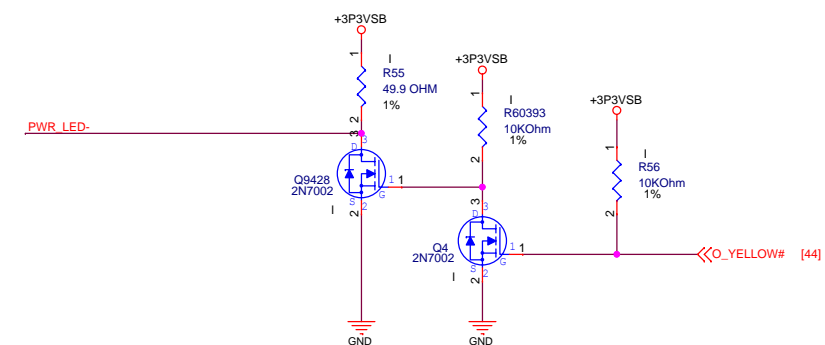
Date: Friday, January 17, 2014 Sheet 53 of 97

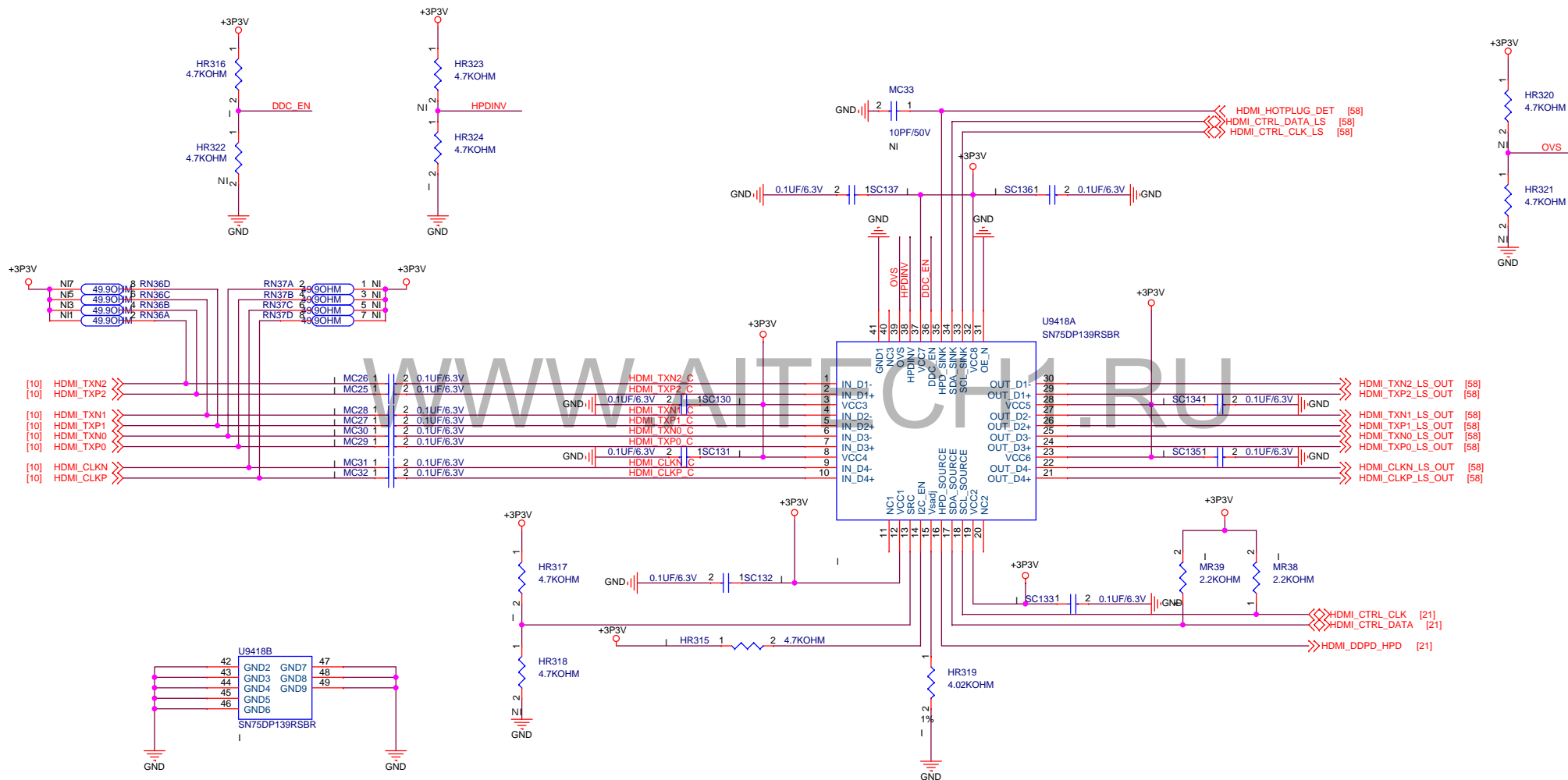
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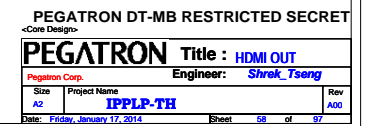
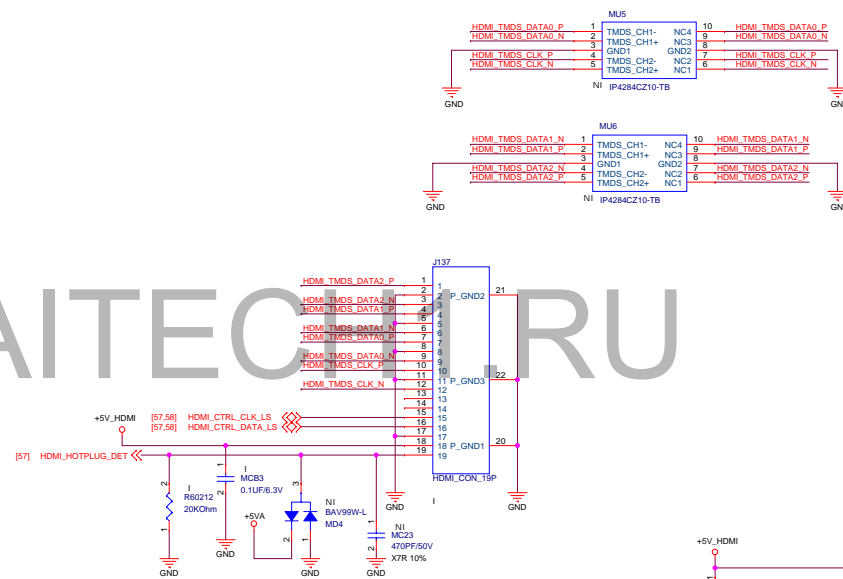
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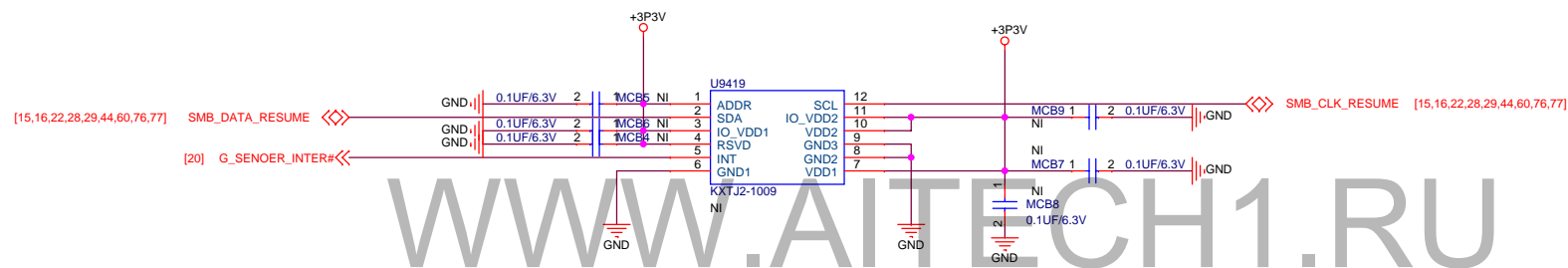
Size A3	Project Name IPPLP-TH	Rev A00
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Date: Friday, January 17, 2014 Sheet 54 of 97



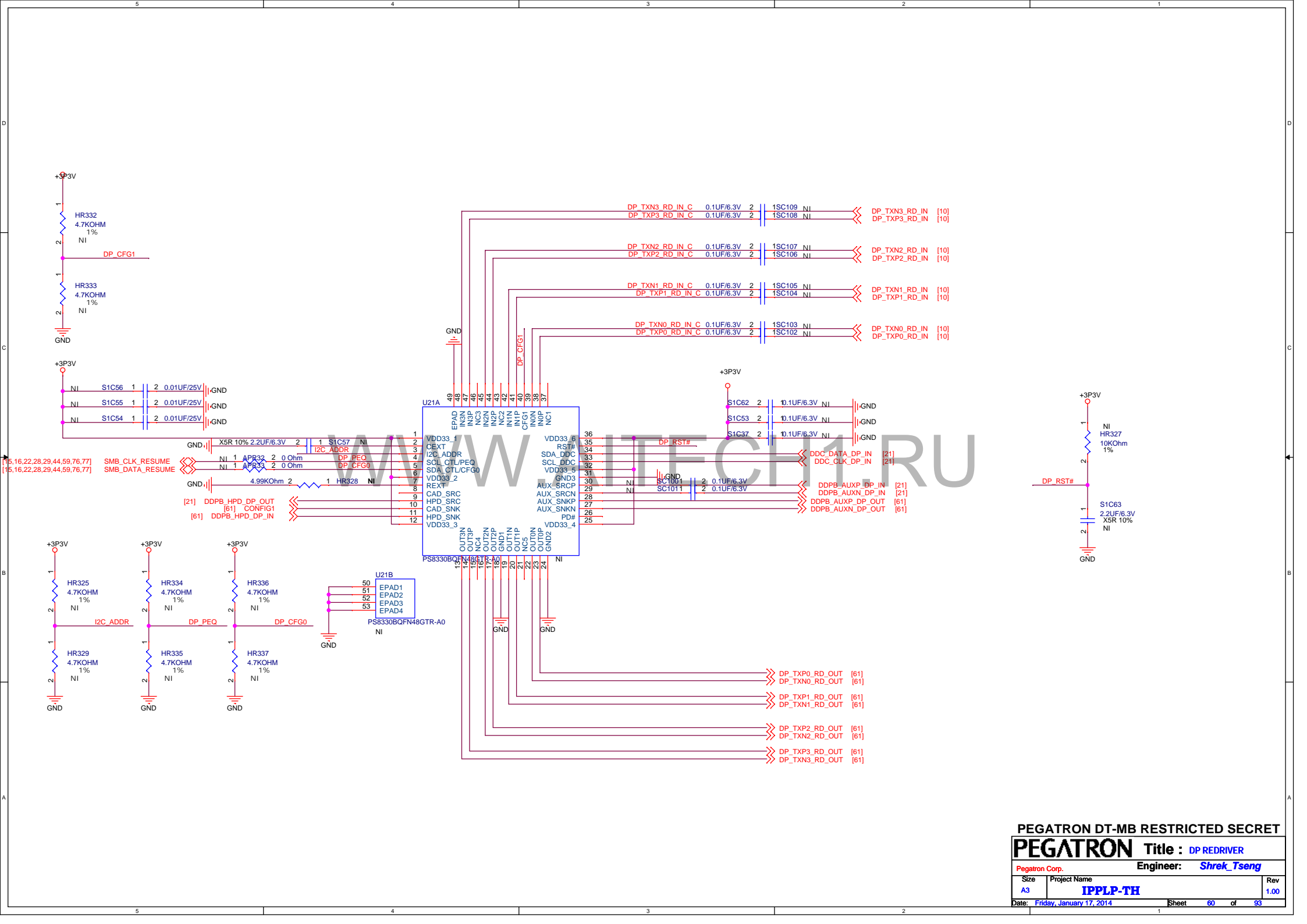






PEGATRON DT-MB RESTRICTED SECRET
<Core Design>

PEGATRON		Title : G-SENSOR	
Pegatron Corp.		Engineer: Shrek Tseng	
Size A3	Project Name IPPLP-TH		Rev A00
Date: Friday, January 17, 2014	Sheet	59	of 97



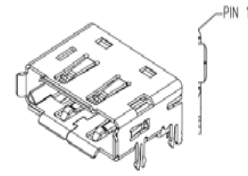
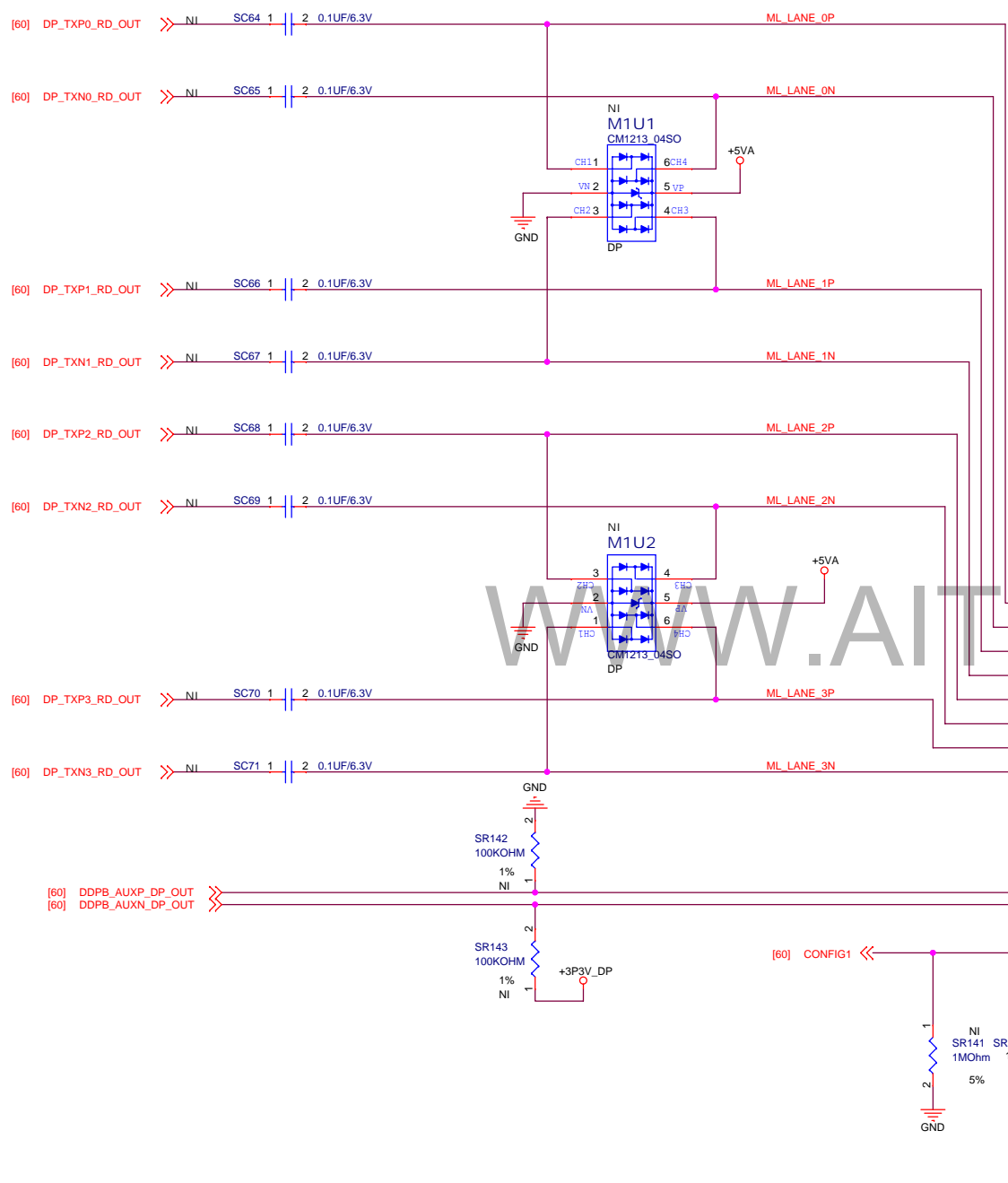
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DP REDRIVER

Pegatron Corp. Engineer: Shrek_Tseng

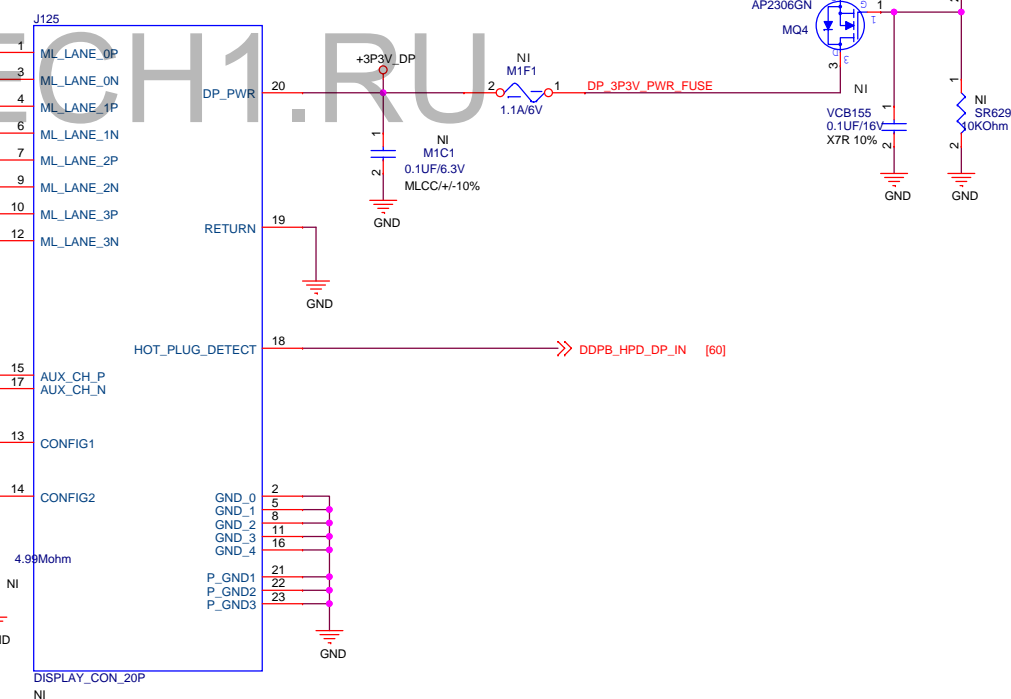
Size	Project Name	Rev
A3	IPPLP-TH	1.00

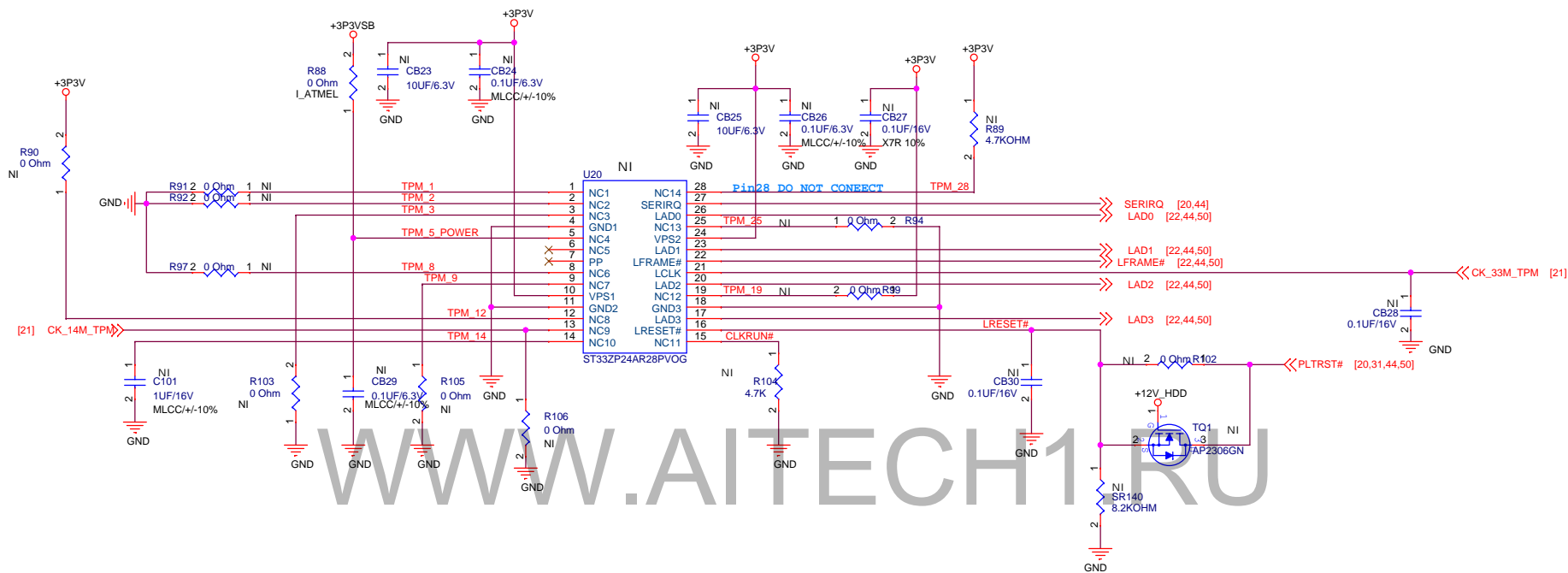
Date: Friday, January 17, 2014 Sheet 60 of 93



NOTE:
Install M1Q6 and M1R7
on Intel Ibox Peak platform

Pass gate to prevent back-drive
when sink device is on and
PCH is powered down





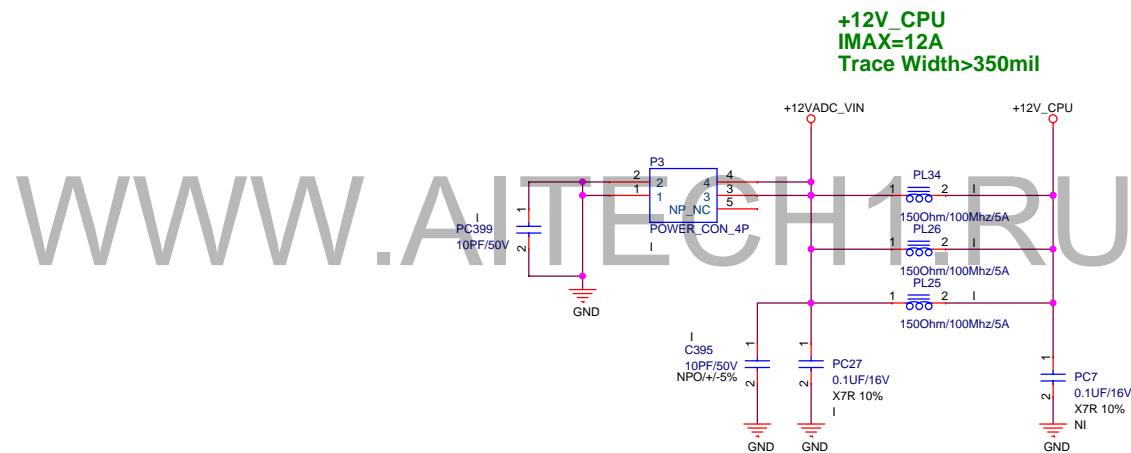
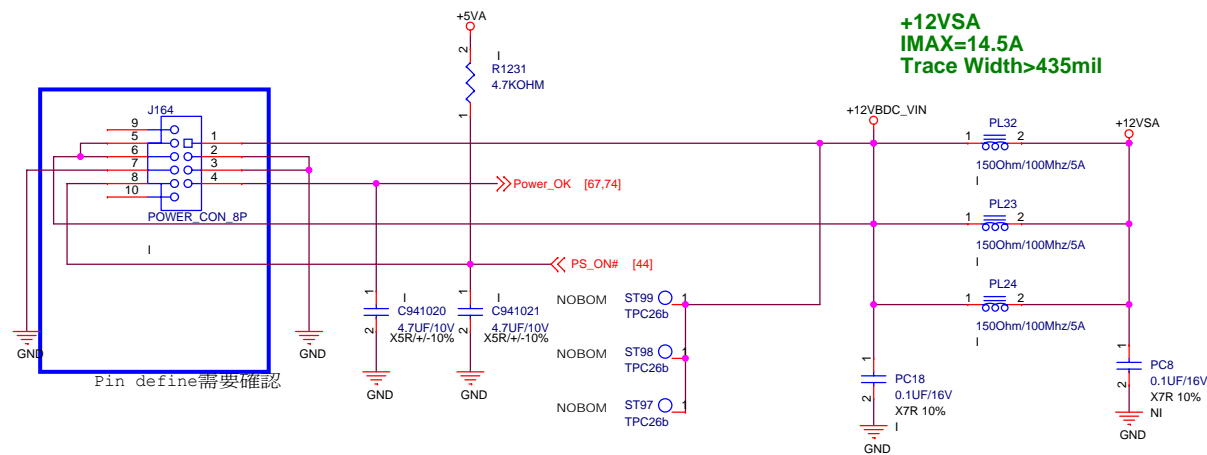
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PEGATRON Title : TPM

Pegatron Corp. Engineer: Shrek Tseng

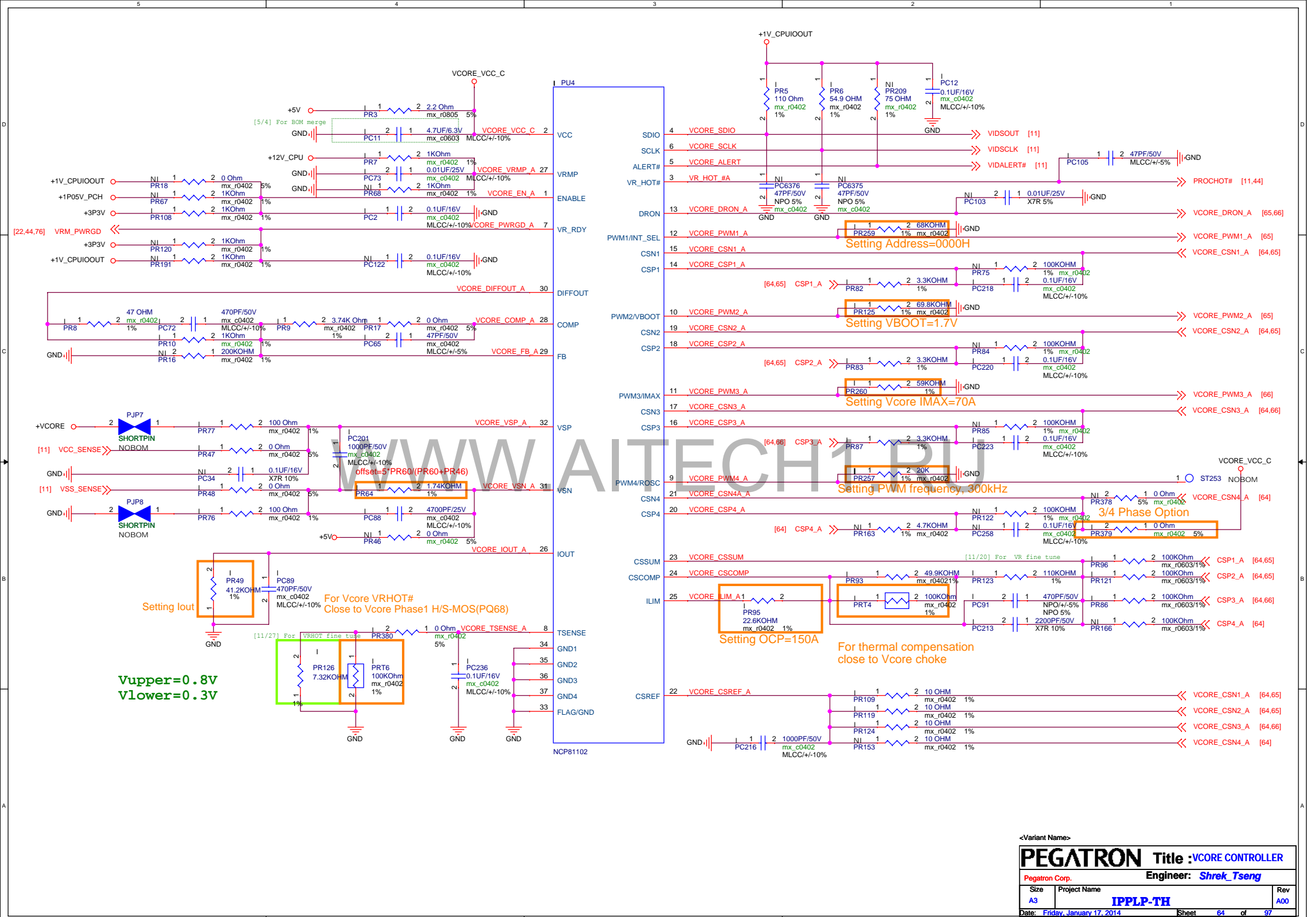
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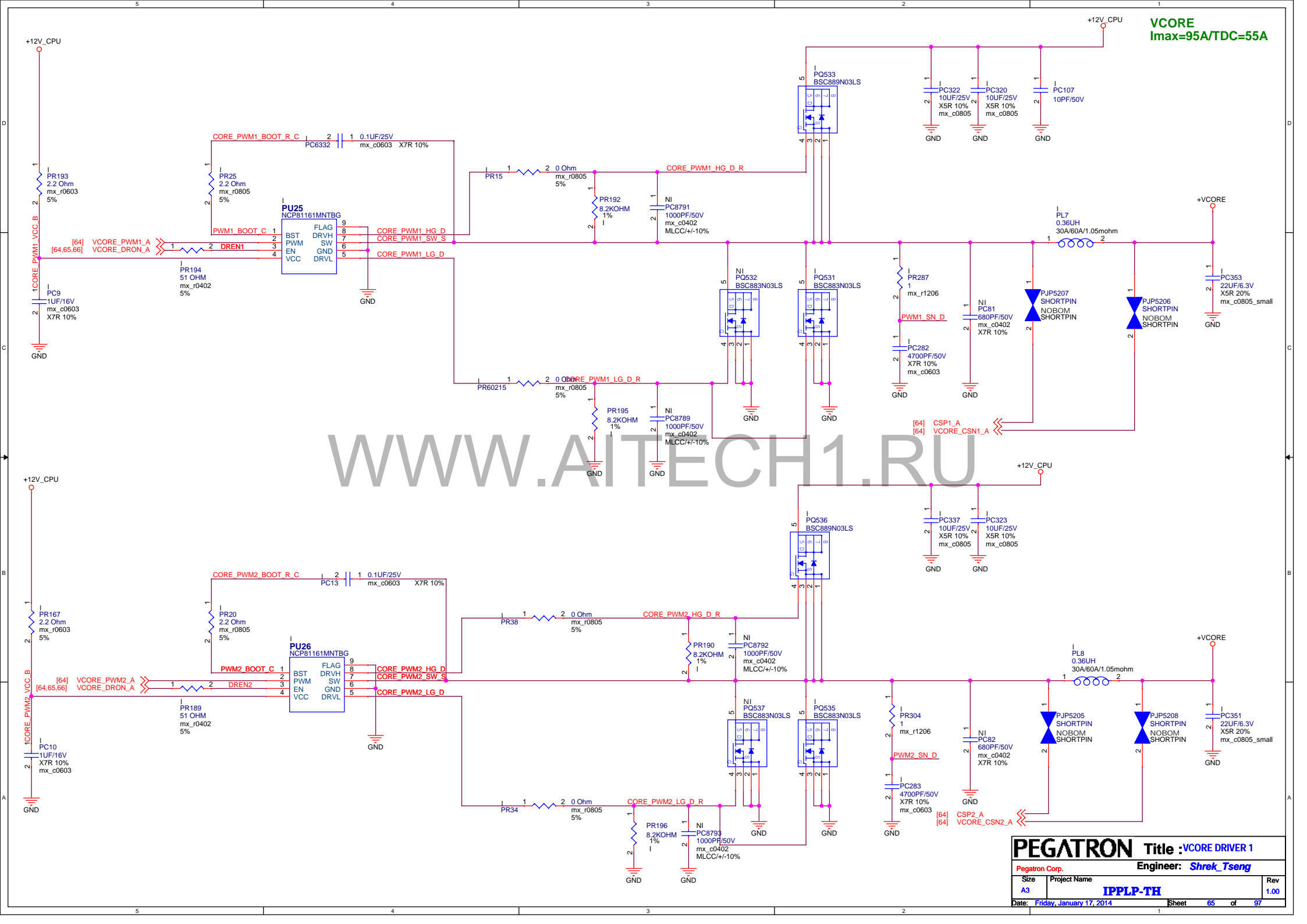
Date: Friday, January 17, 2014 Sheet 62 of 97



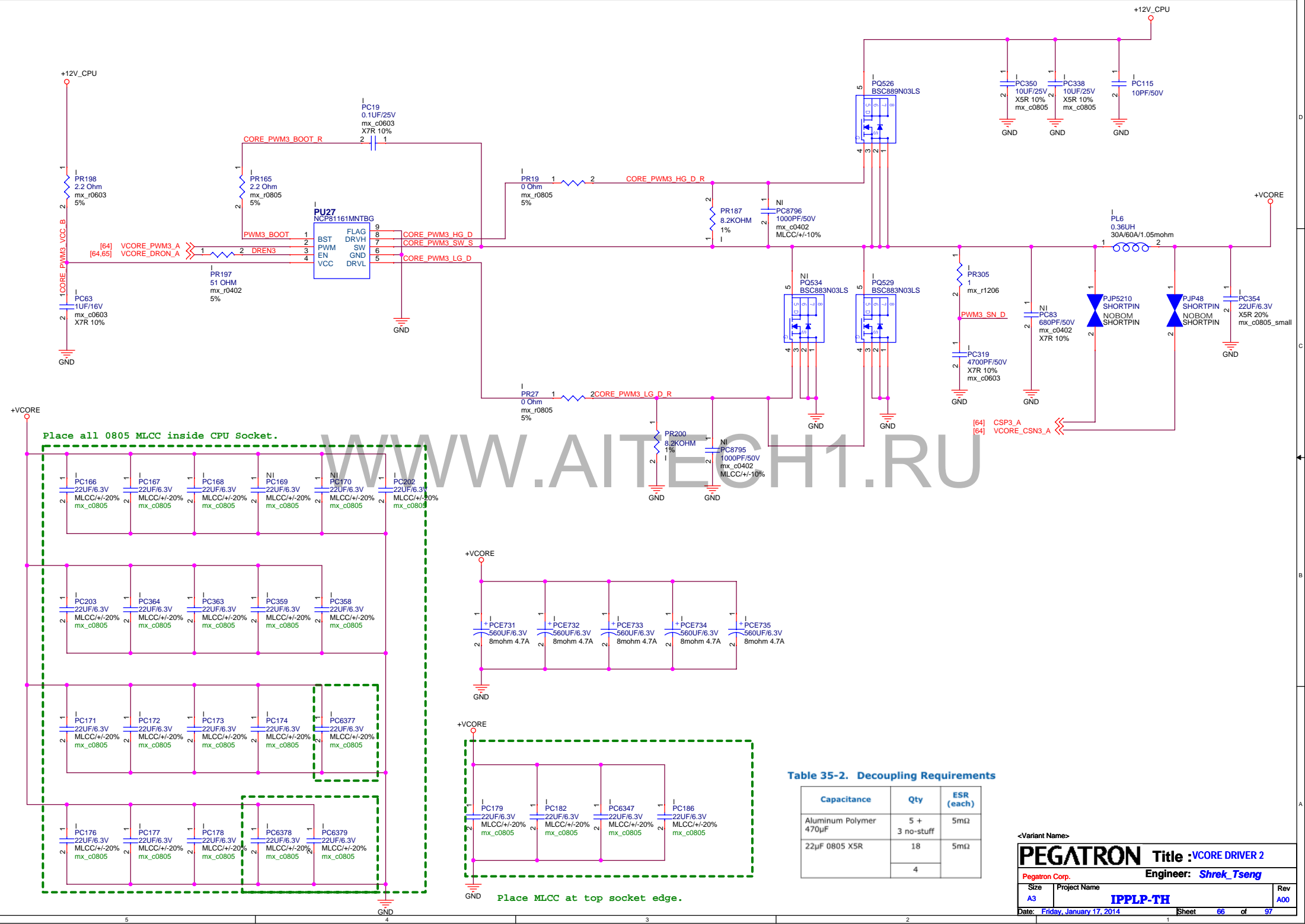
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : DC IN	
Pegatron Corp.		Engineer: Shrek_Tseng	
Size A3	Project Name IPPLP-TH		Rev A00
Date: Friday, January 17, 2014		Sheet 63	of 97





VCORE
I_{max}=95A/TDC=55A



Place all 0805 MLCC inside CPU Socket.

Place MLCC at top socket edge.

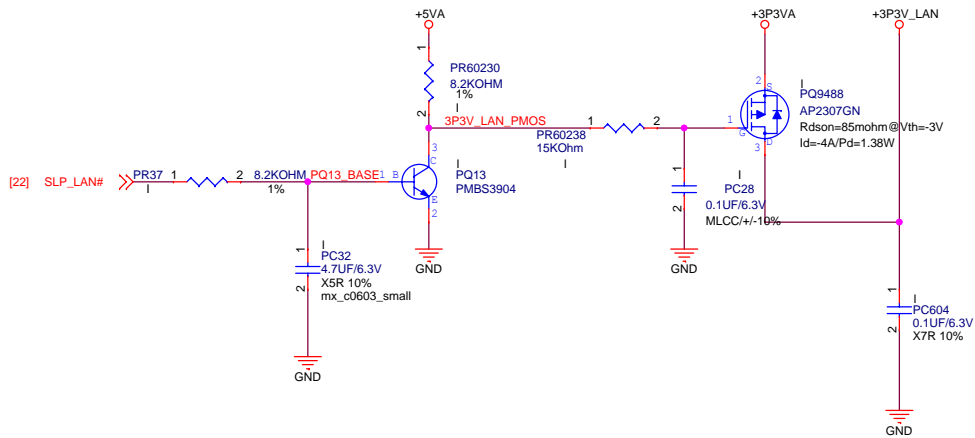
Table 35-2. Decoupling Requirements

Capacitance	Qty	ESR (each)
Aluminum Polymer 470µF	5 + 3 no-stuff	5mΩ
22µF 0805 X5R	18	5mΩ
	4	

<Variant Name>

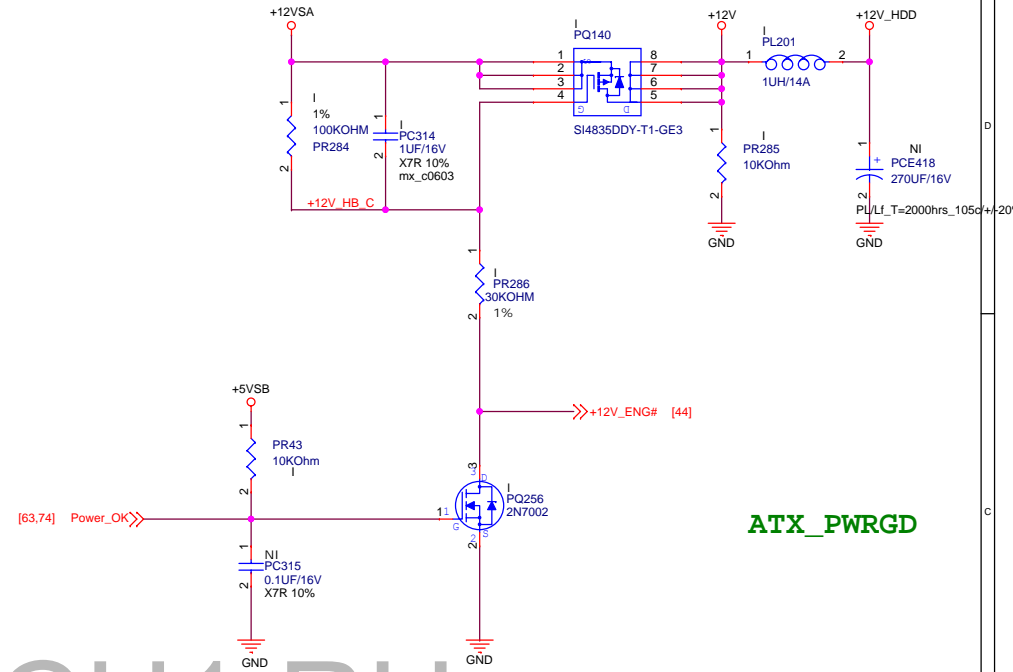
+3.3V_LAN

Imax=0.188A
Vdroop: 0.188A*218mohm=40mV



+12V/Imax:10A/TDC:7A

Vdroop: 7A*18mohm=126mV

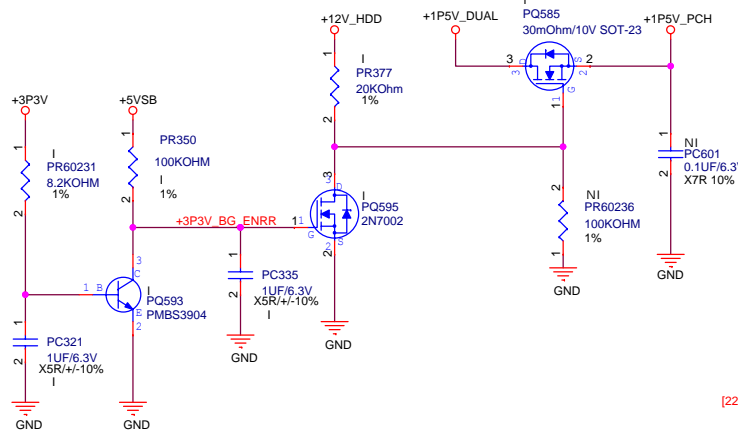


ATX_PWRGD

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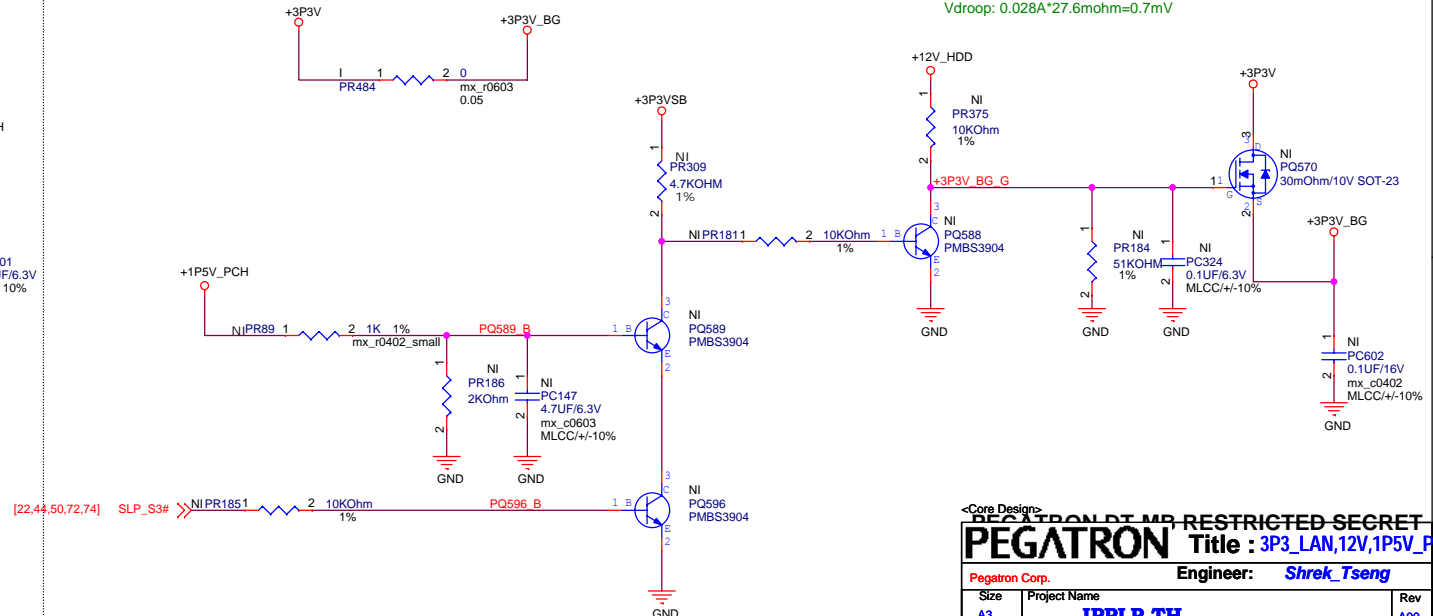
+1P5V_PCH/Imax:0.36A

Vdroop: 0.36A*27.6mohm=19mV

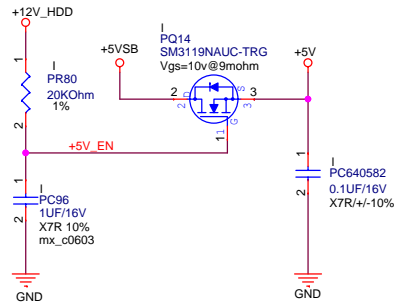


+3P3V_BG/Imax:0.028A

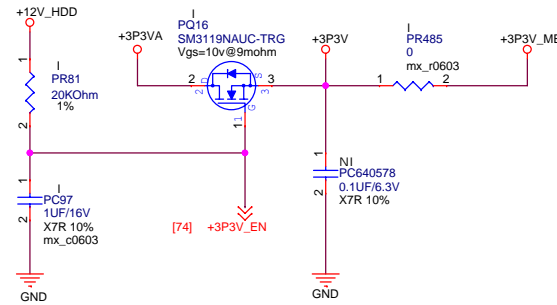
Vdroop: 0.028A*27.6mohm=0.7mV



+5V / I_{max}: 6.42A / TDC: 4.5A
Vdroop: 4.5A*9mohm=40.5mV



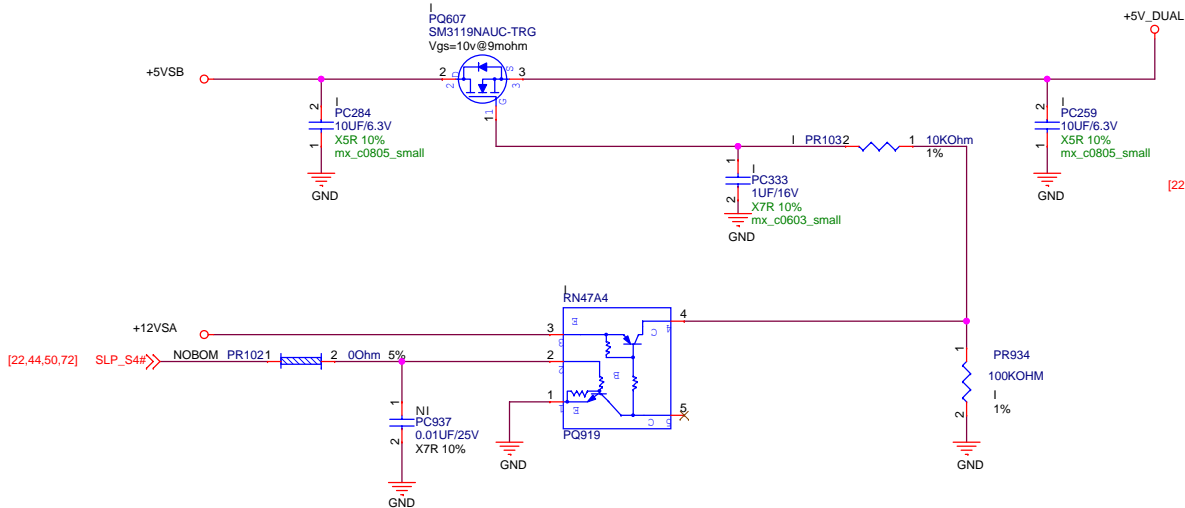
+3P3V / I_{max}: 8.57A / TDC: 6A
Vdroop: 6A*9mohm=54mV



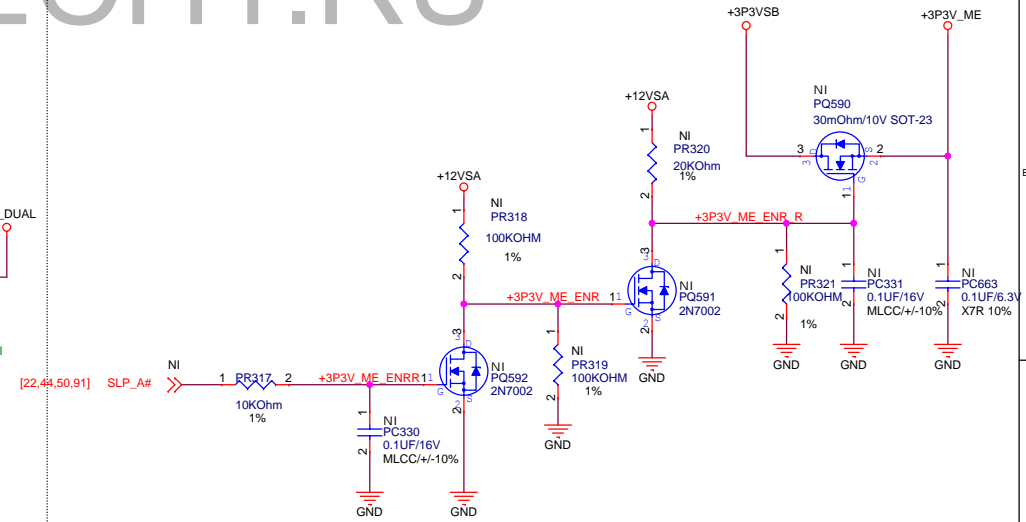
WWW.AITECH1.RU

+5V_DUAL / TDC: 8.5A

Vdroop = 8.5A*13.8m = 117mV



+3P3V_ME / I_{max}: 0.03A
Vdroop: 0.03A*27.6mohm=1mV



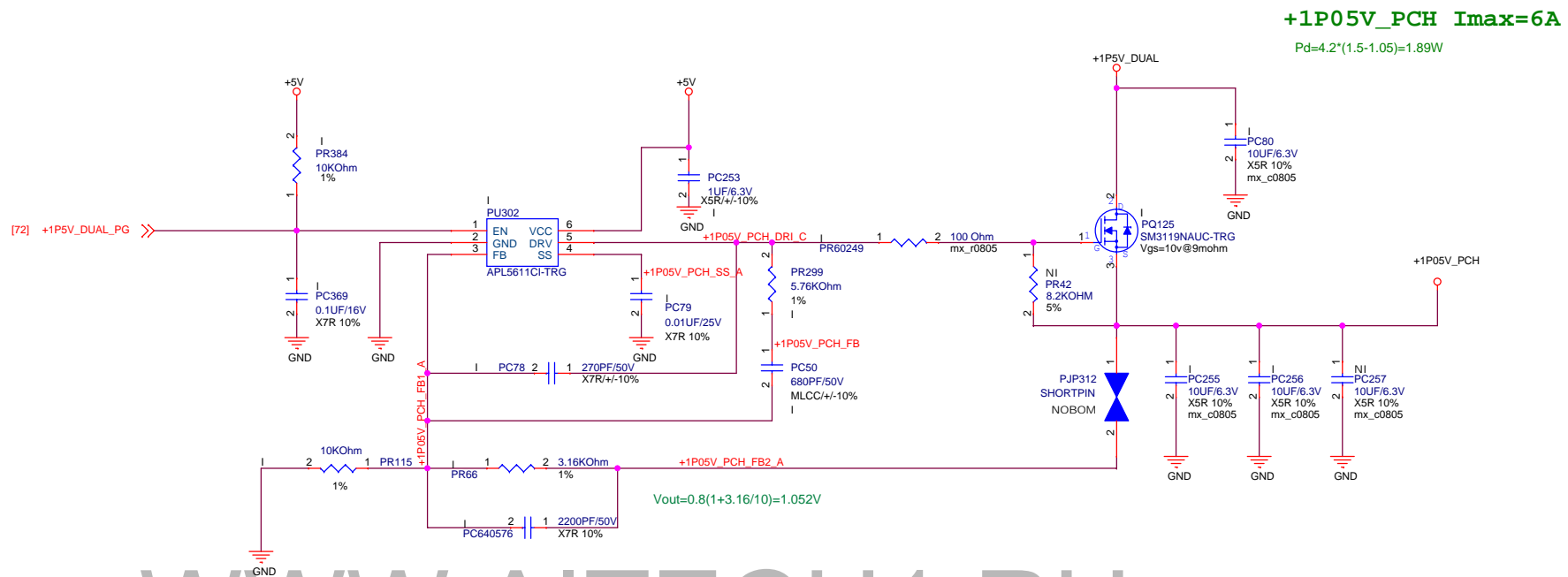
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 5V, 3P3V, 1P5V, 5V_Dual

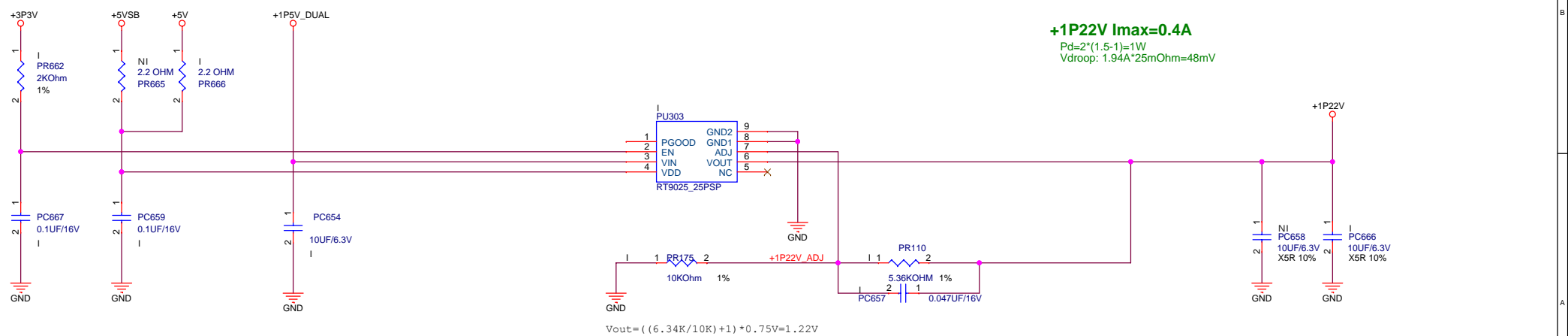
Pegatron Corp. Engineer: Shrek Tseng

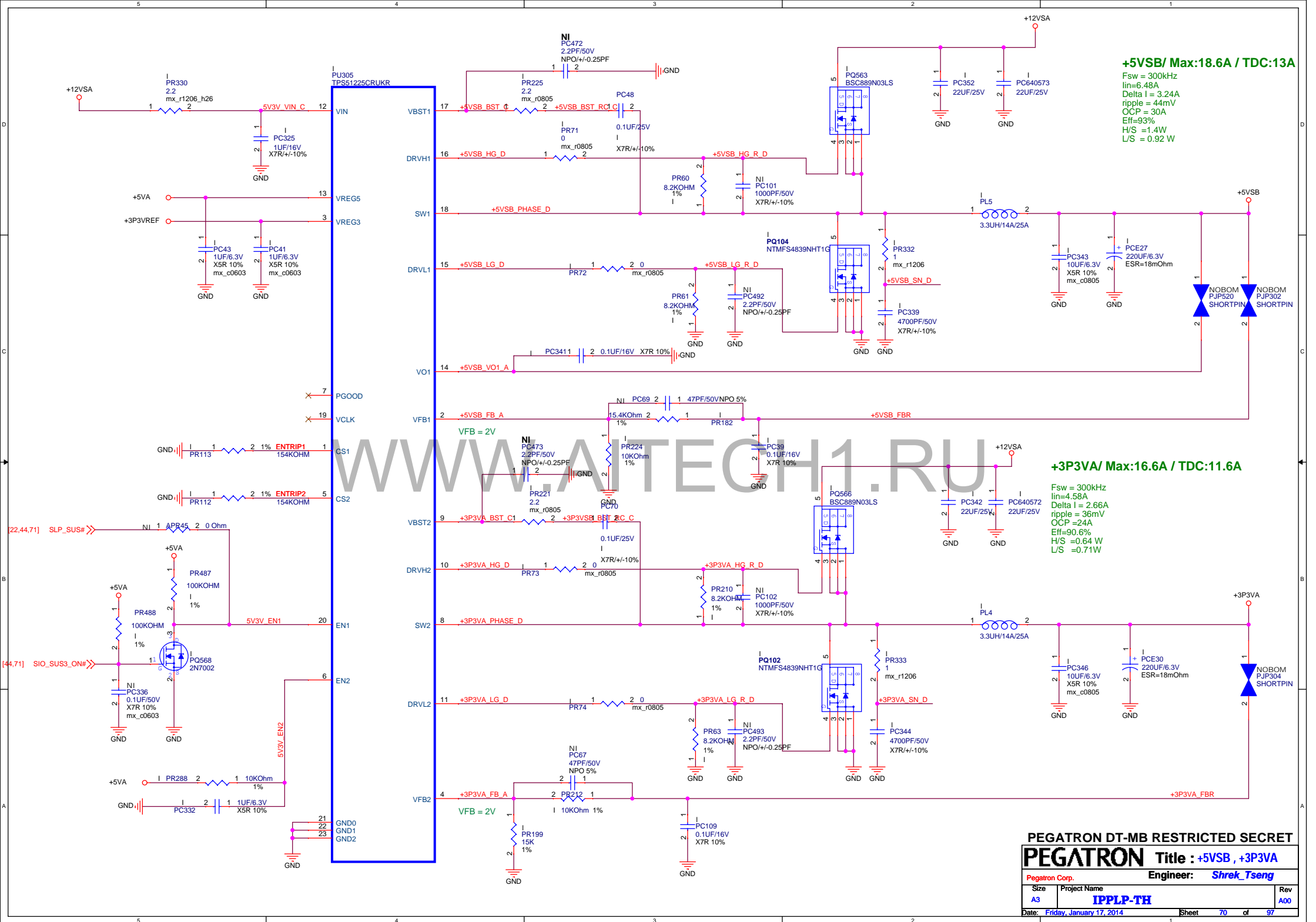
Size A3 Project Name IPPLP-TH Rev A00

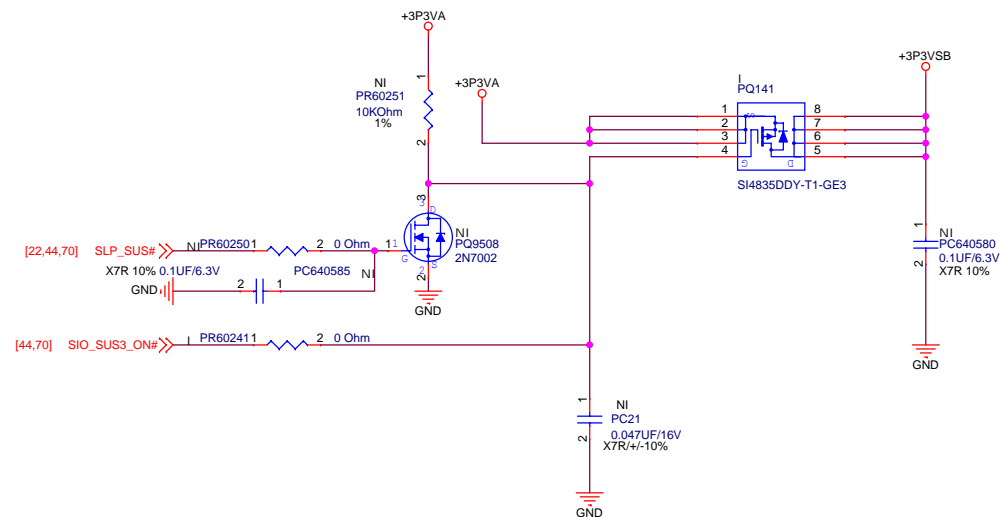
Date: Friday, January 17, 2014 Sheet 68 of 97



WWW.AITECH1.RU

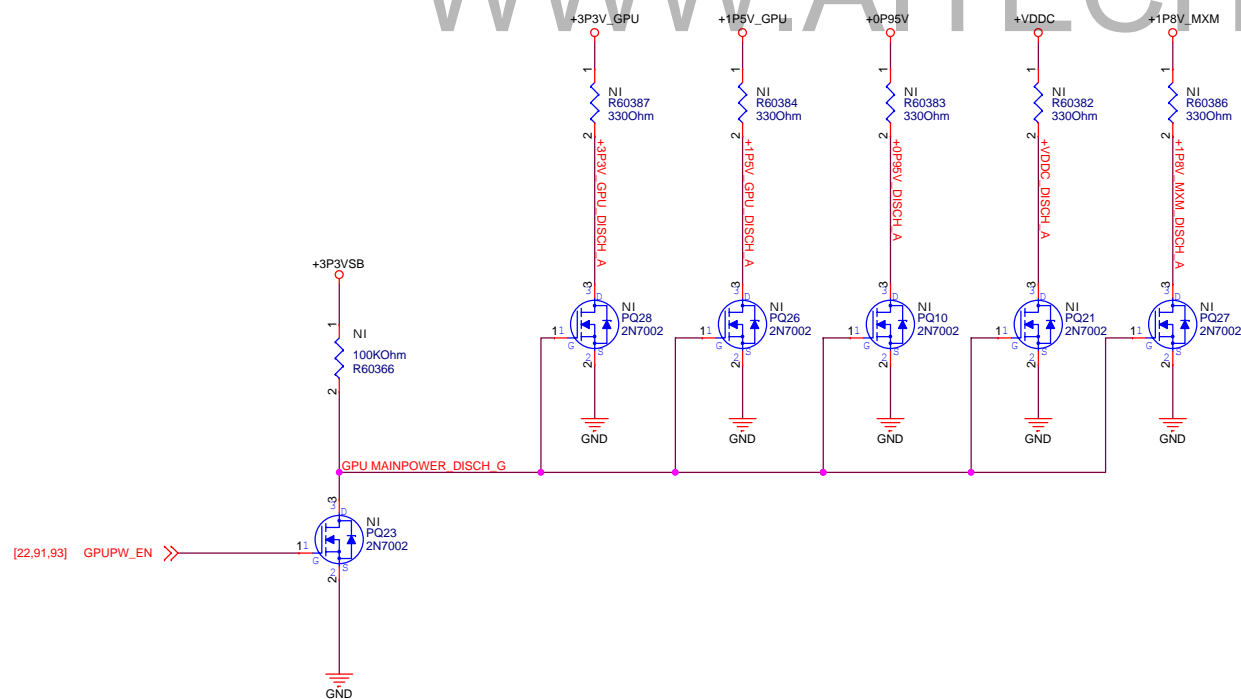






GPU POWER DISCHARGE

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<Variant Name>

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Pegatron Corp.			Engineer: Shrek_Tseng	
Size A3	Project Name IPPLP-TH			Rev A00
Date: Friday, January 17, 2014		Sheet 71 of 97		

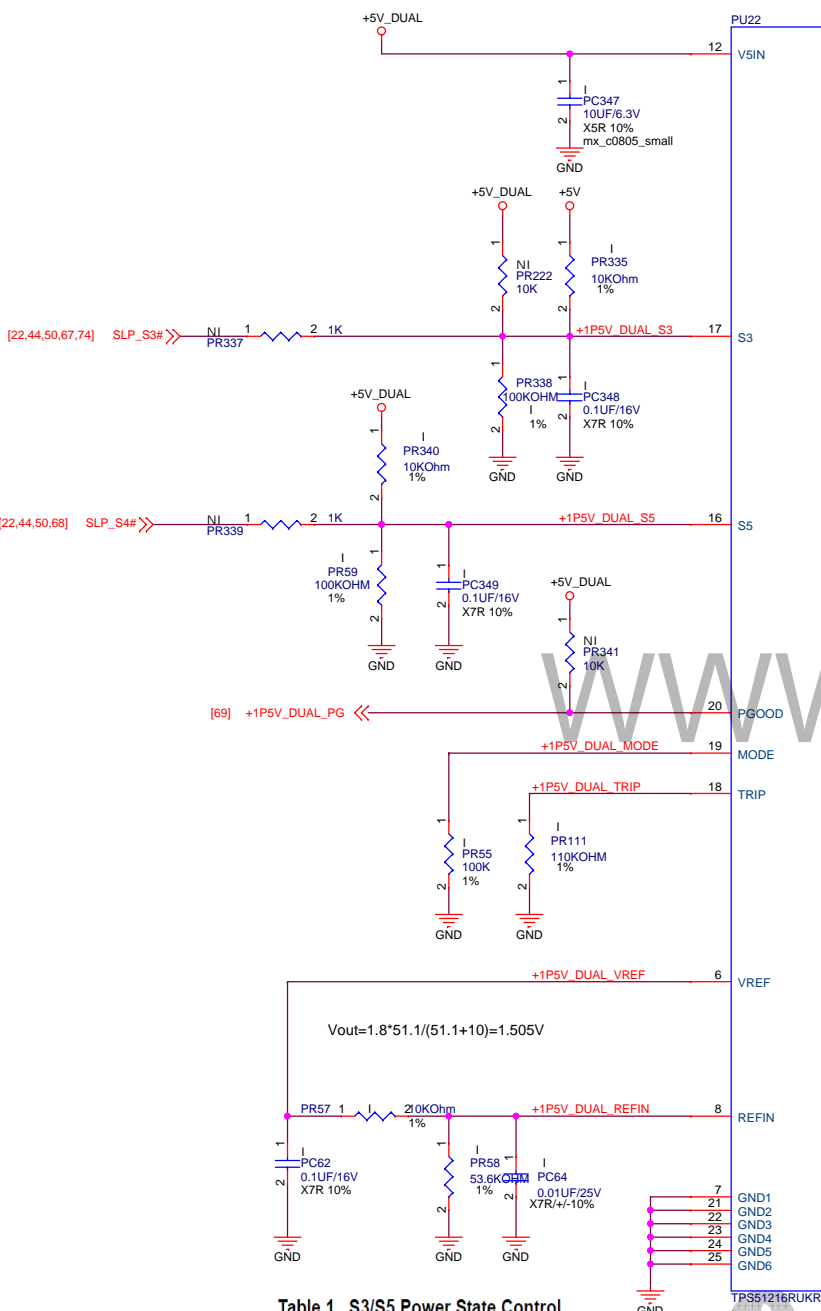
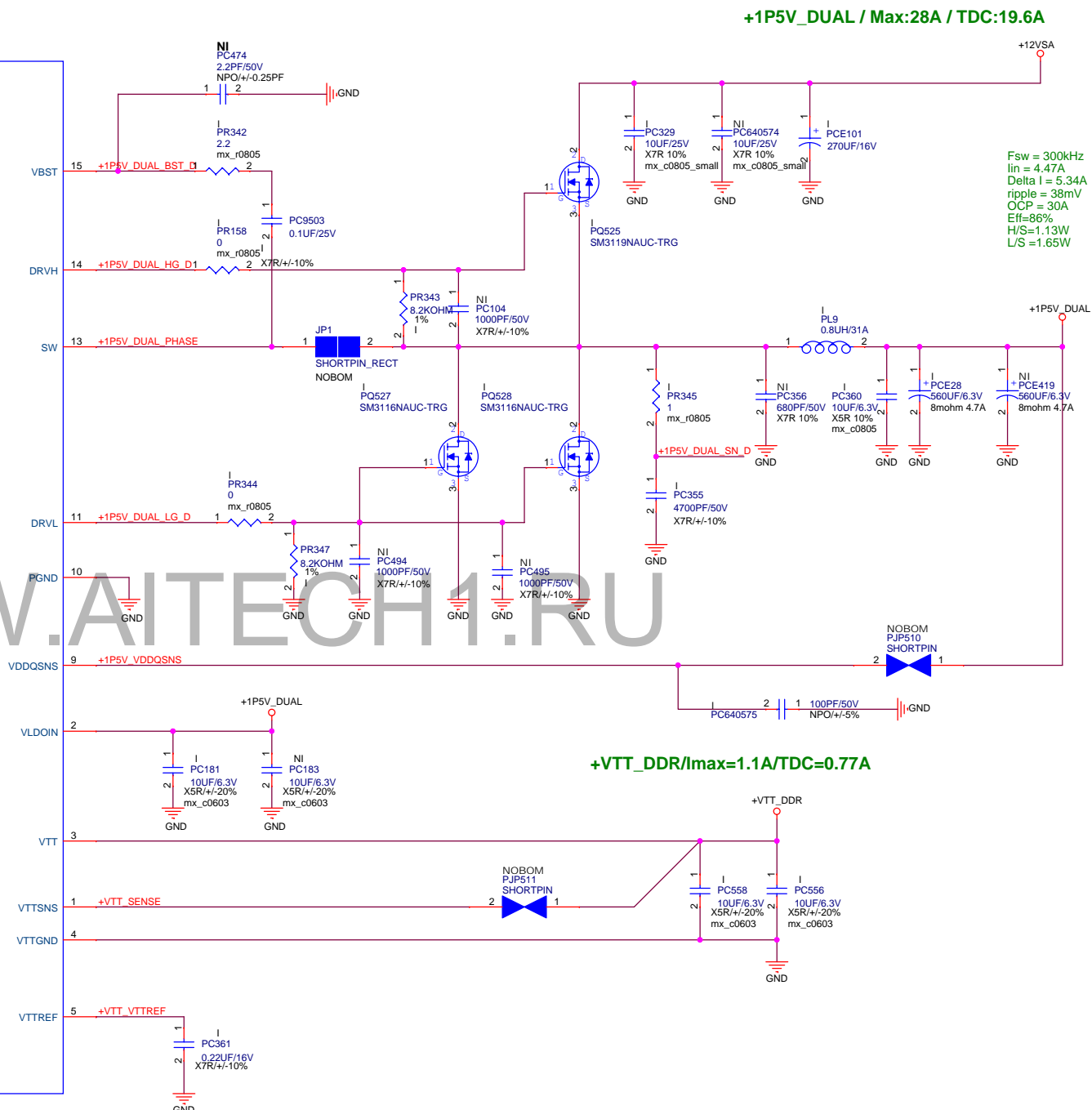


Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

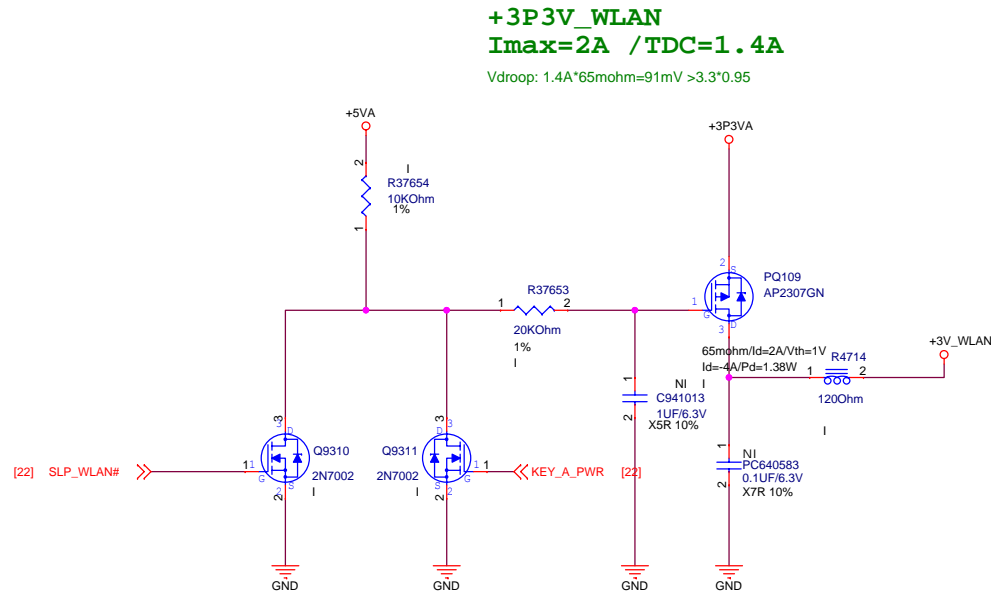


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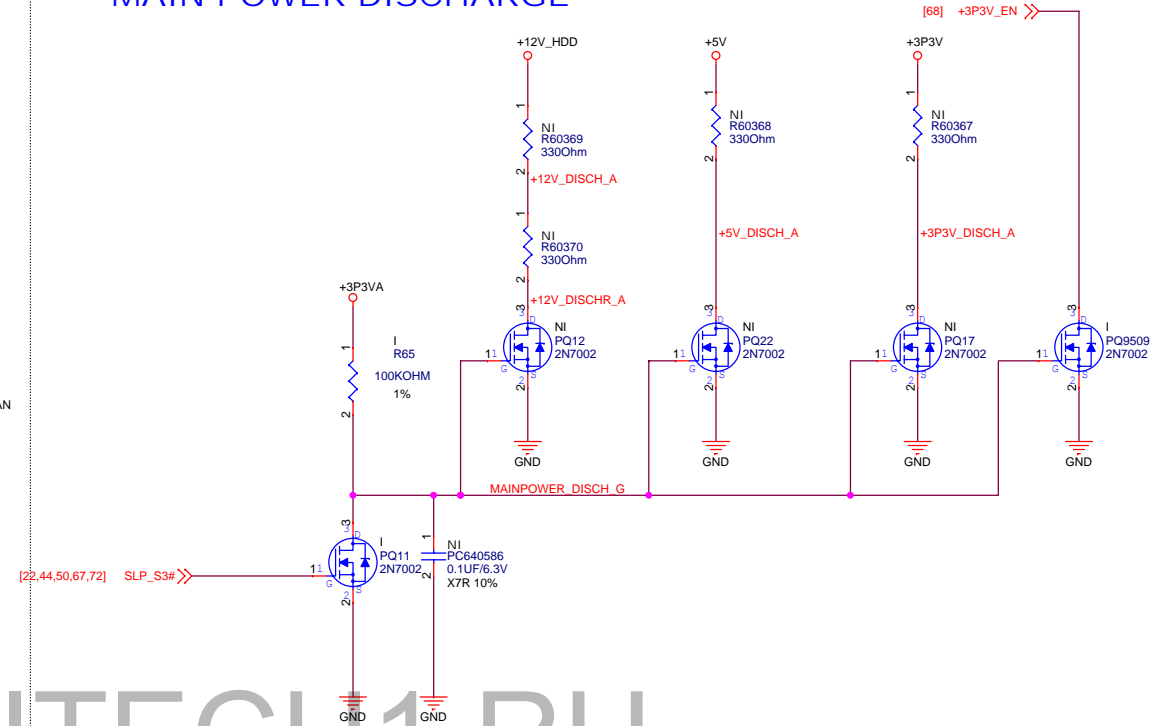
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PEGATRON DT-MB RESTRICTED SECRET

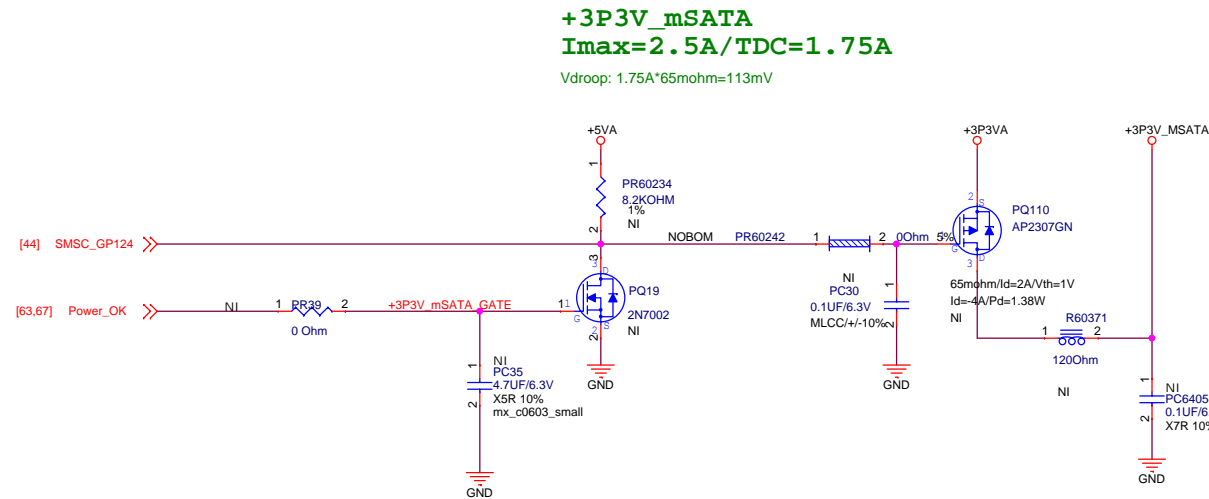
PEGATRON		Title : XXXXX
Pegatron Corp.		Engineer: Shrek_Tseng
Size A3	Project Name IPPLP-TH	Rev A00
Date: Friday, January 17, 2014		Sheet 73 of 97



MAIN POWER DISCHARGE



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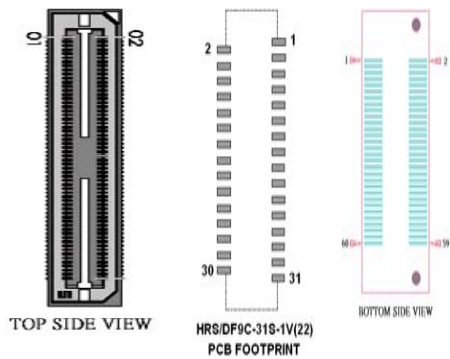
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PEGATRON DT-MB RESTRICTED SECRET

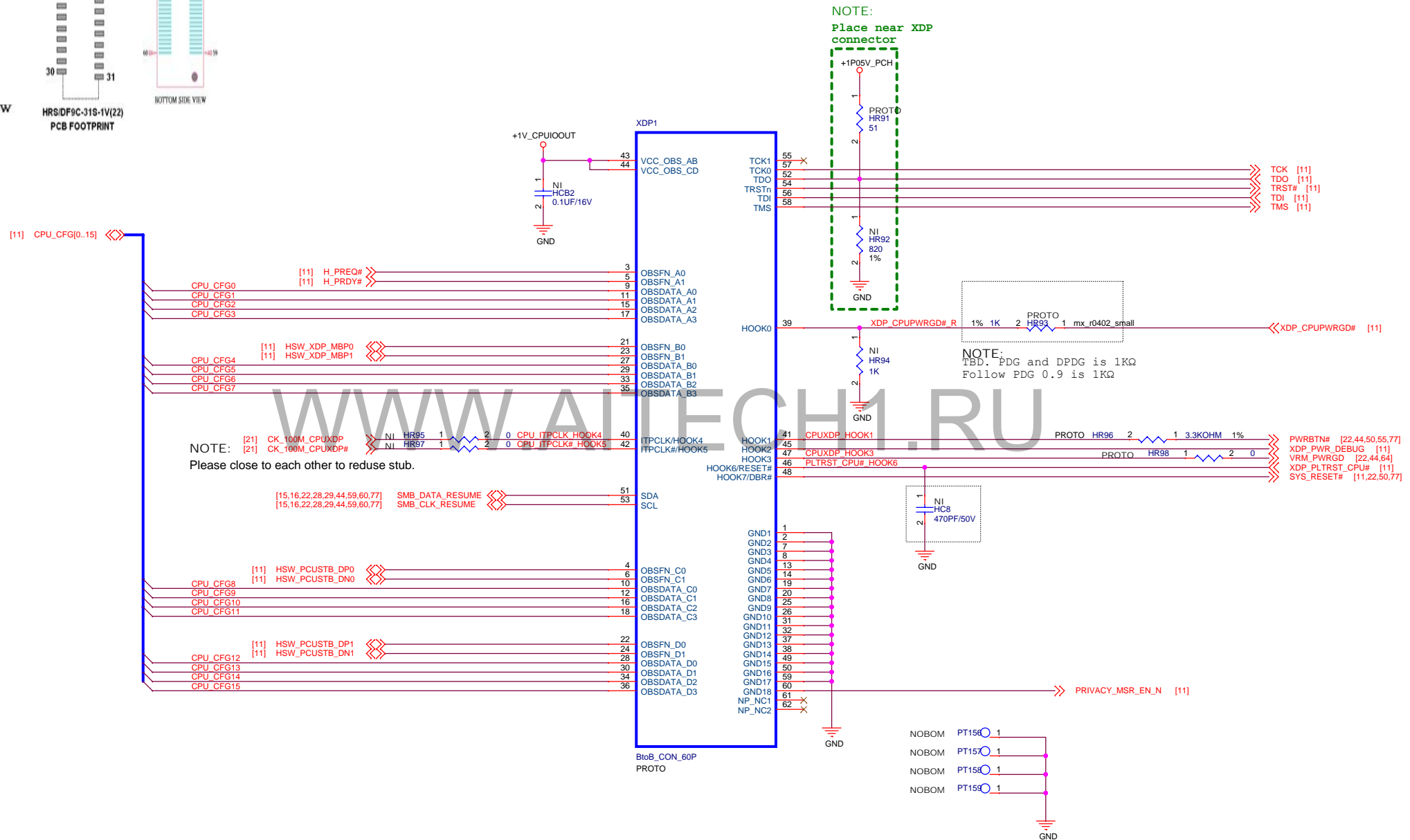
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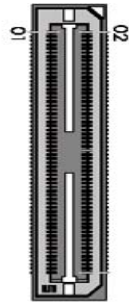
Pegatron Corp. Engineer: Shrek_Tseng

Size A3	Project Name IPPLP-TH	Rev A00
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INTEL CPU XDP DEBUG PORT

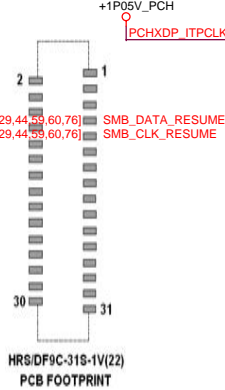
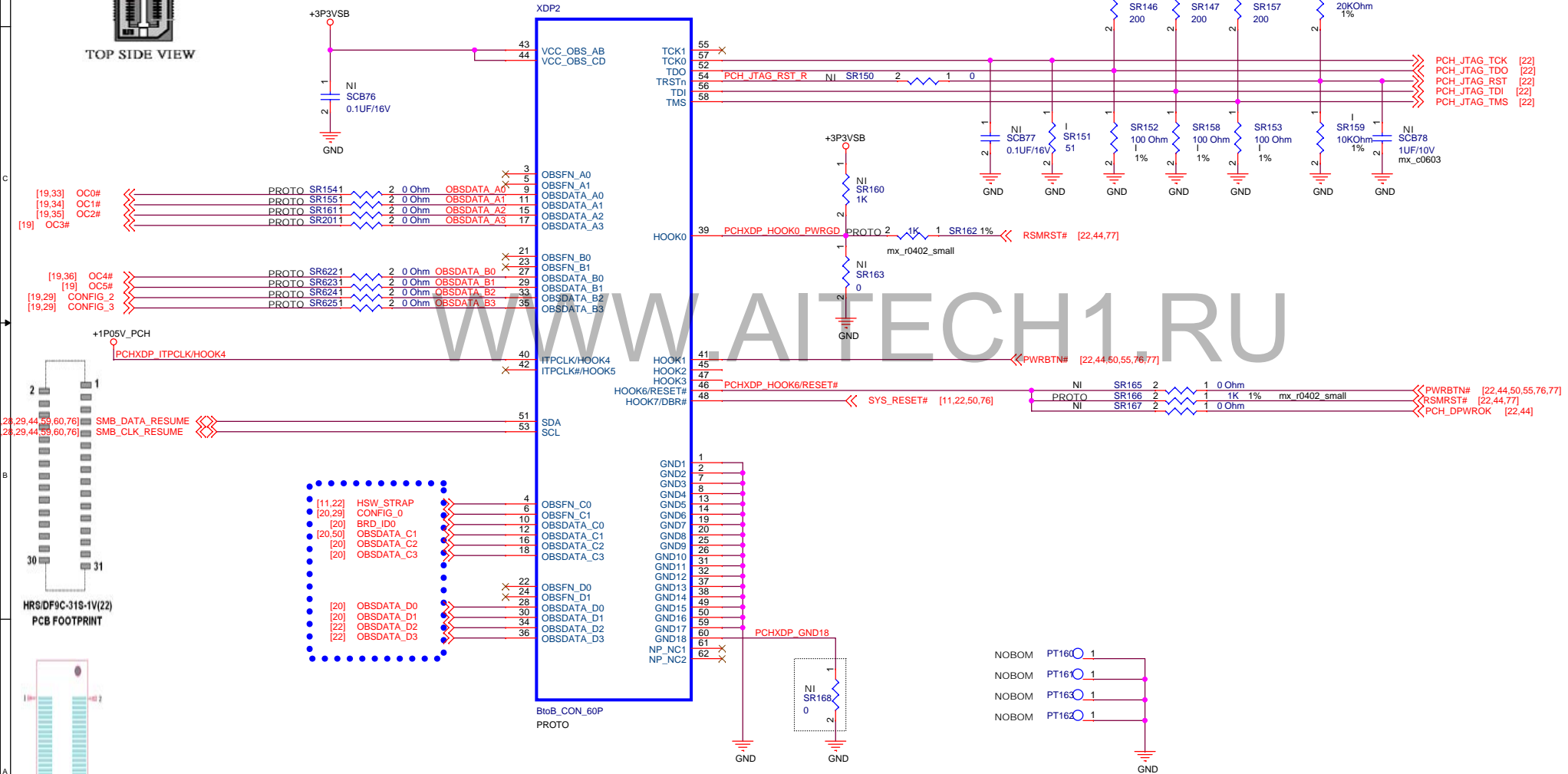




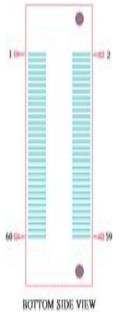
TOP SIDE VIEW

INTEL PCH XDP DEBUG PORT

NOTE:
Place strap resistors of TDO near to XDP connector,
and TDI and TMS near to CPU.



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT

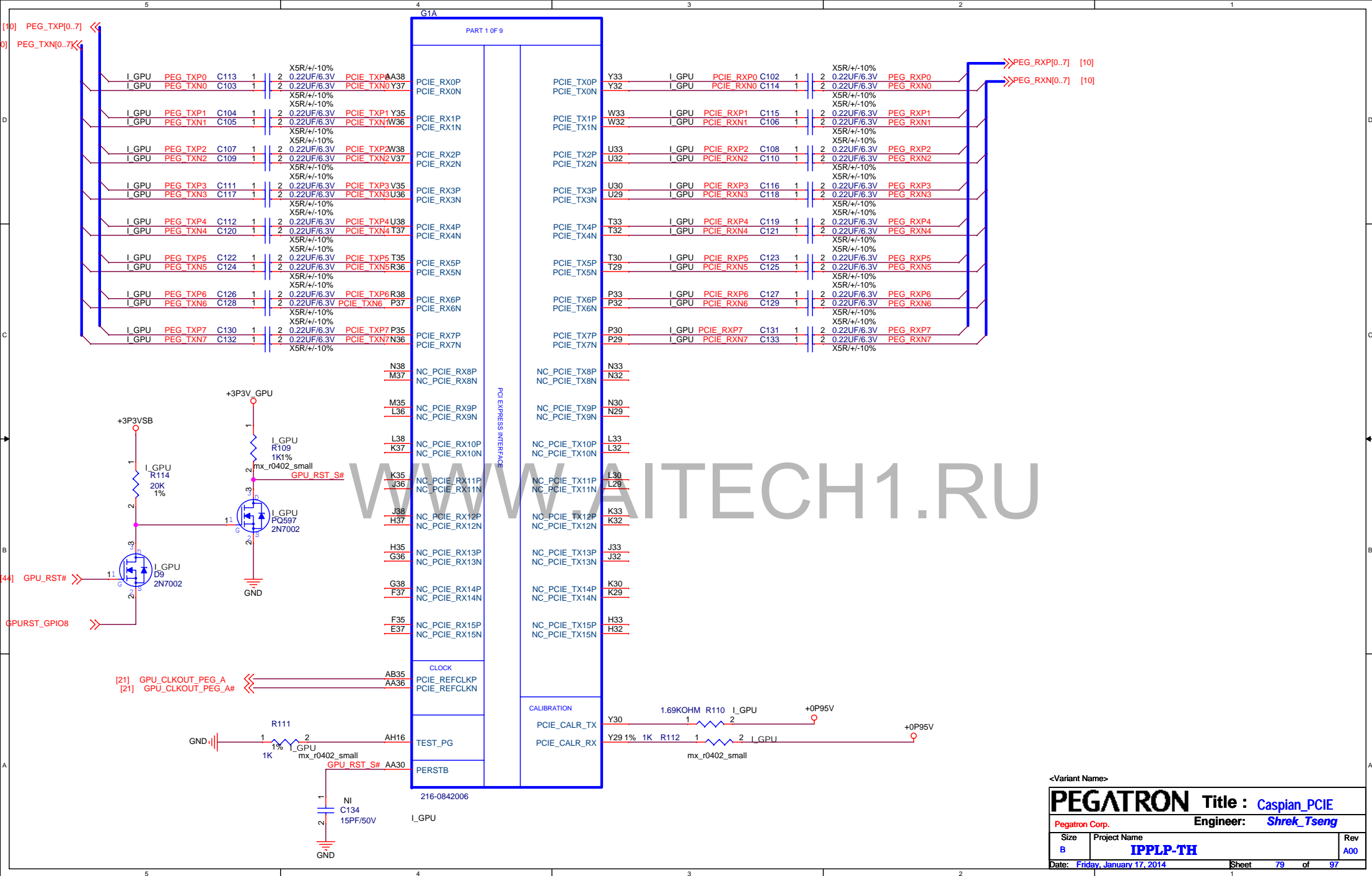


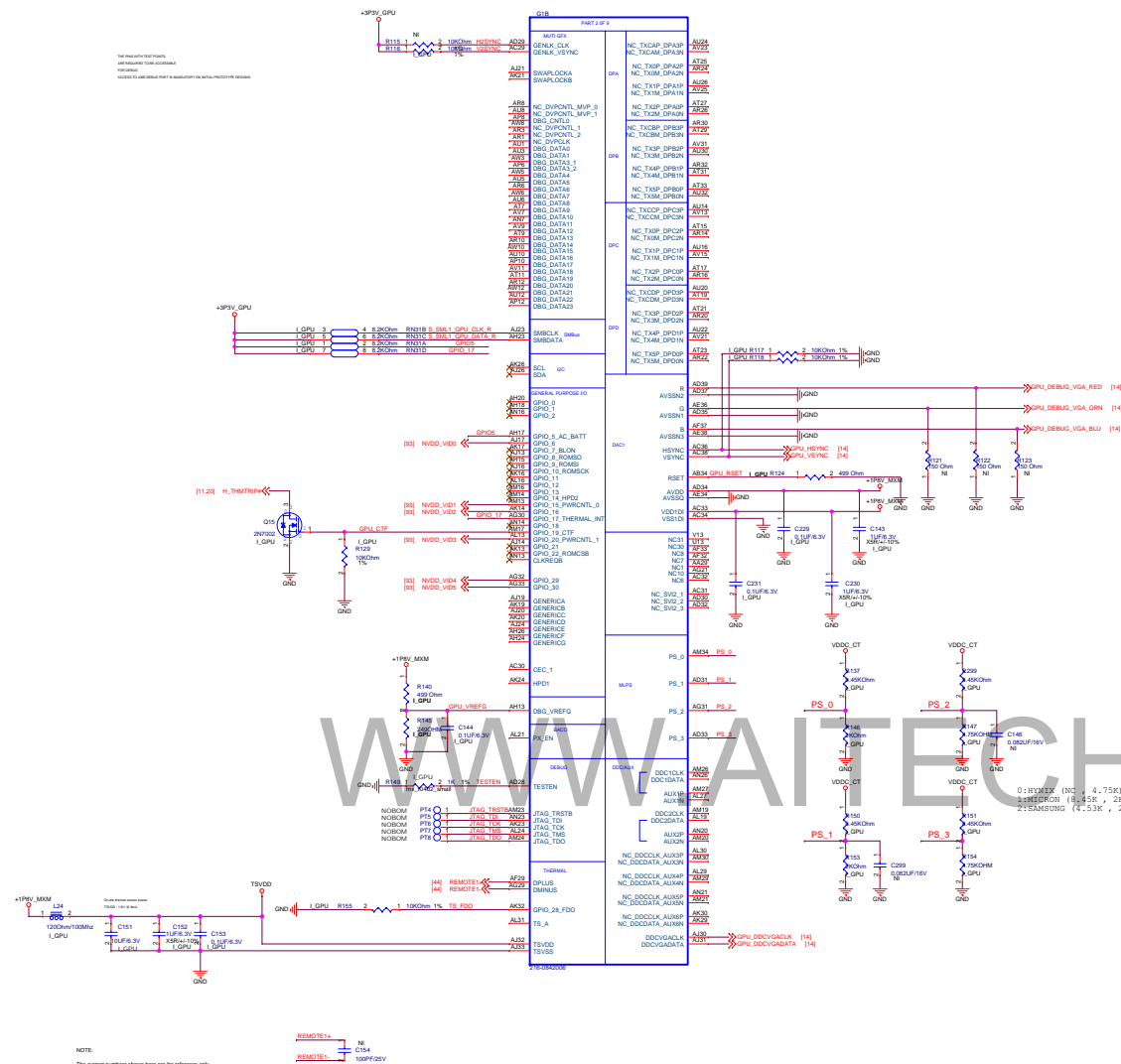
BOTTOM SIDE VIEW

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : XXXXXX	
Pegatron Corp.		Engineer: Shrek Tseng	
Size A3	Project Name IPPLP-TH		Rev A00
Date: Friday, January 17, 2014		Sheet 78 of 97	





COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

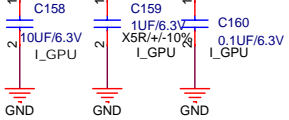
For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

For Thames/Whistler/Seymour
a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

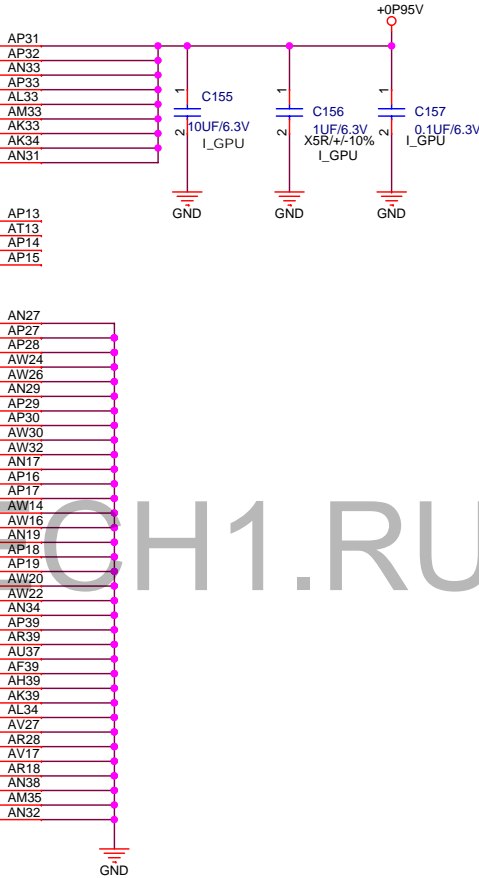
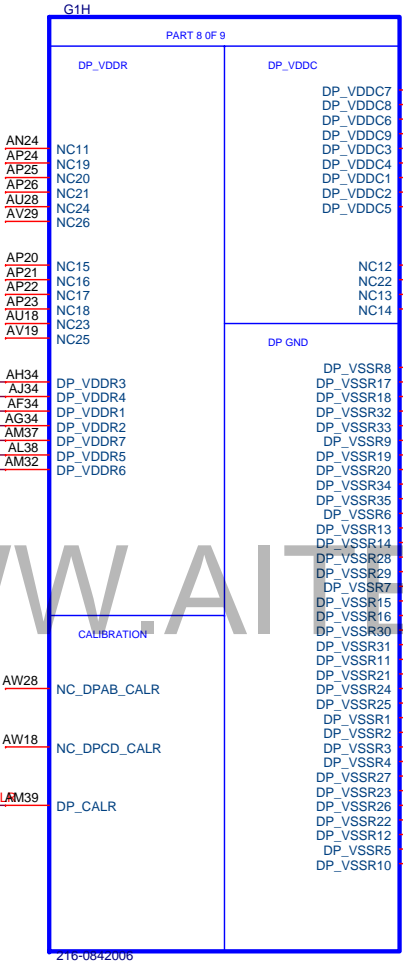
DP/TMDSLVDS Transmitter Power
DP mode: 1.8V @ 188mA per port
HDMI mode: 1.8V @ 237mA per port

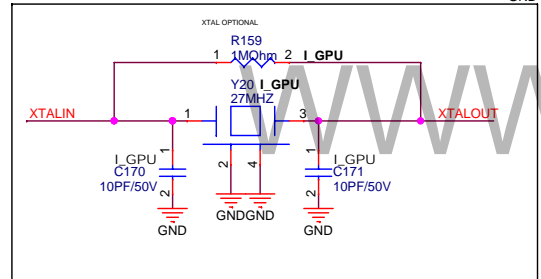
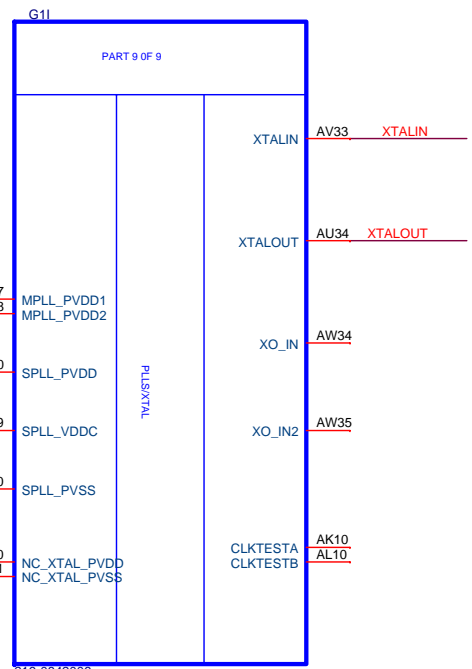
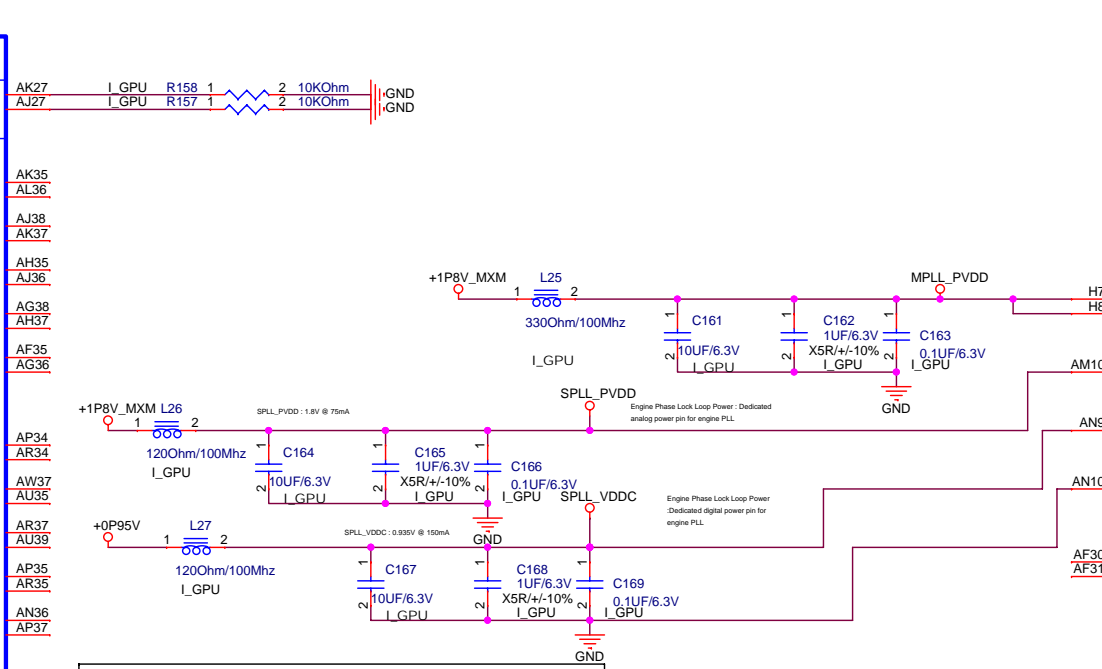
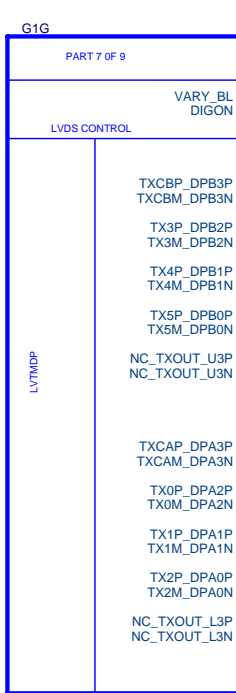
DP/TMDSLVDS Transmitter Power
0.935V @ 222mA per port

+1P8V_MXM



NOTE:
The current numbers shown here are for reference only
For actual current, check with databook



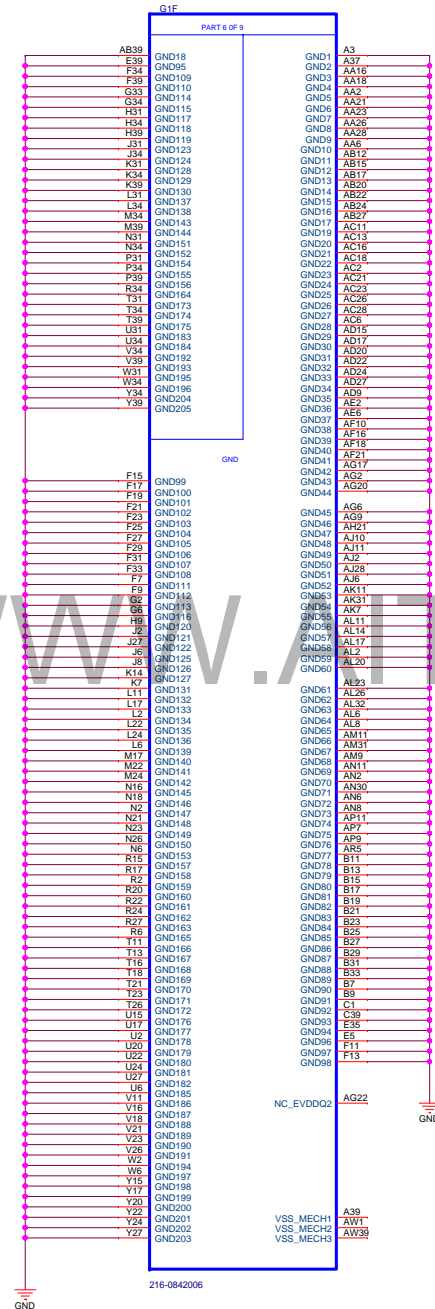


216-0842006

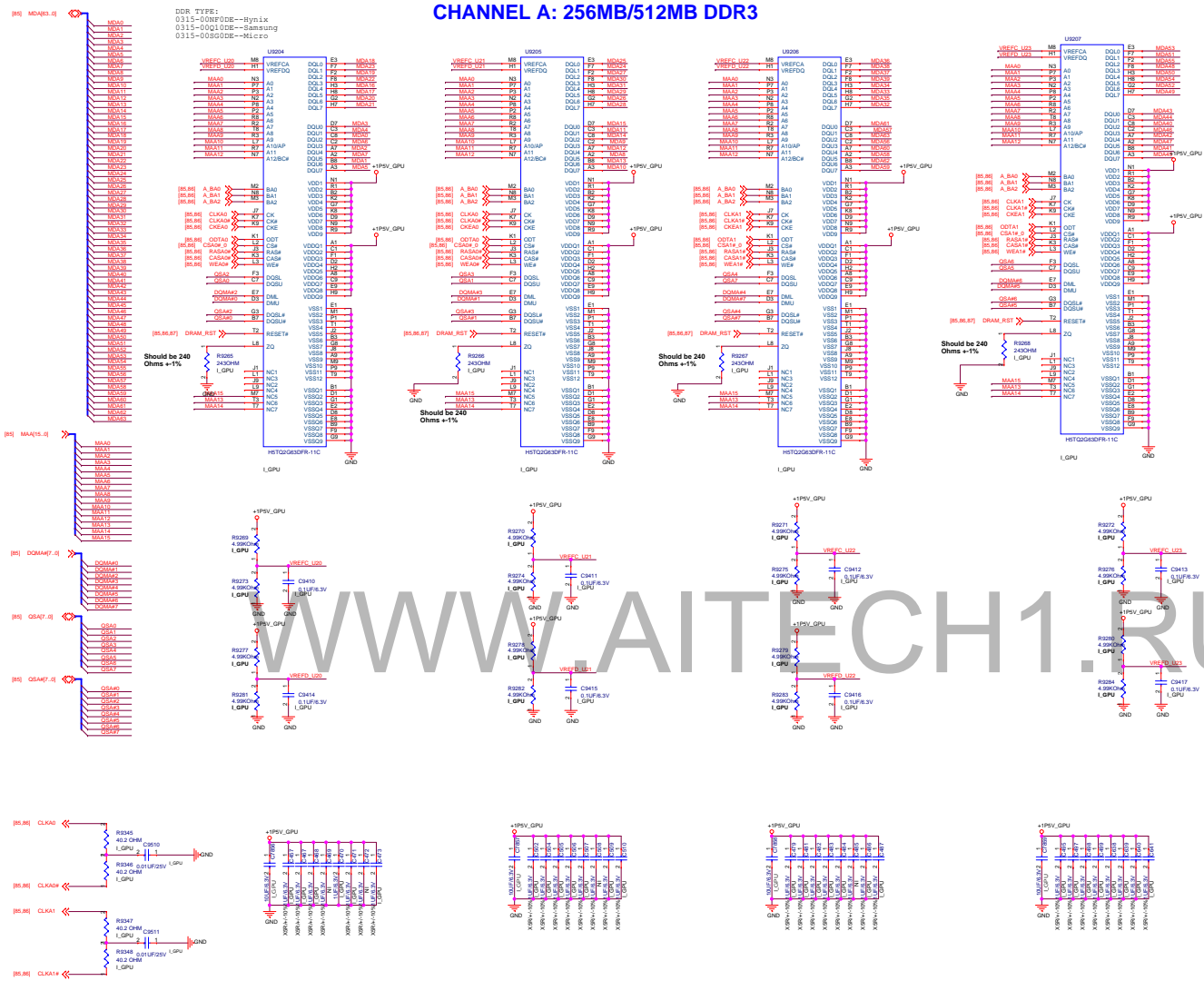
<Variant Name>		Title : Caspian_LVDS1	
Pegatron Corp.		Engineer: Shrek_Tseng	
Size B	Project Name IPPLP-TH		Rev A00
Date: Friday, January 17, 2014		Sheet 82 of 97	



COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



CHANNEL A: 256MB/512MB DDR3





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<Variant Name>

PEGATRON		Title : XXXXXX	
Pegatron Corp.		Engineer: Shrek_Tseng	
Size	Project Name	Rev	
A3	IPPLP-TH	A00	
Date: Friday, January 17, 2014		Sheet	88 of 97

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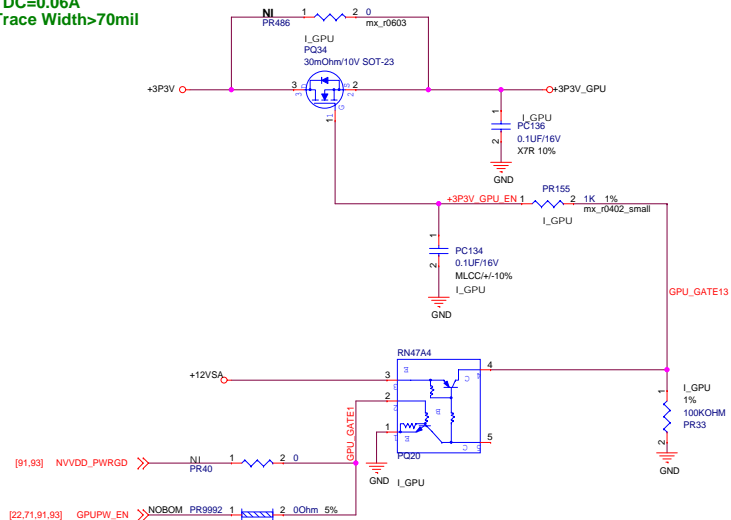
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PEGATRON		Title : XXXXXX	
Pegatron Corp.		Engineer: Shrek_Tseng	
Size	Project Name		Rev
A3	IPPLP-TH		A00
Date: Friday, January 17, 2014		Sheet	89 of 97

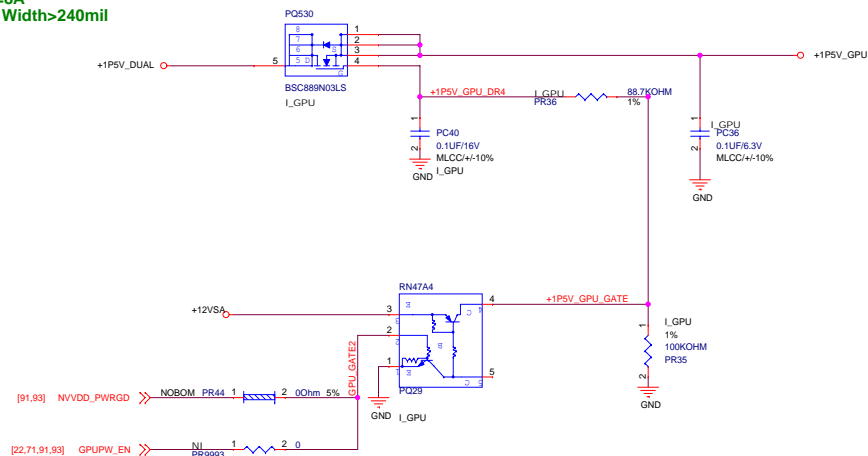
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<Variant Name>		
PEGATRON		Title : XXXXXX
Pegatron Corp.		Engineer: Shrek_Tseng
Size A3	Project Name IPPLP-TH	Rev A00
Date: Friday, January 17, 2014		
Sheet 90 of 97		

+3P3V_GPU
TDC=0.06A
Trace Width>70mil

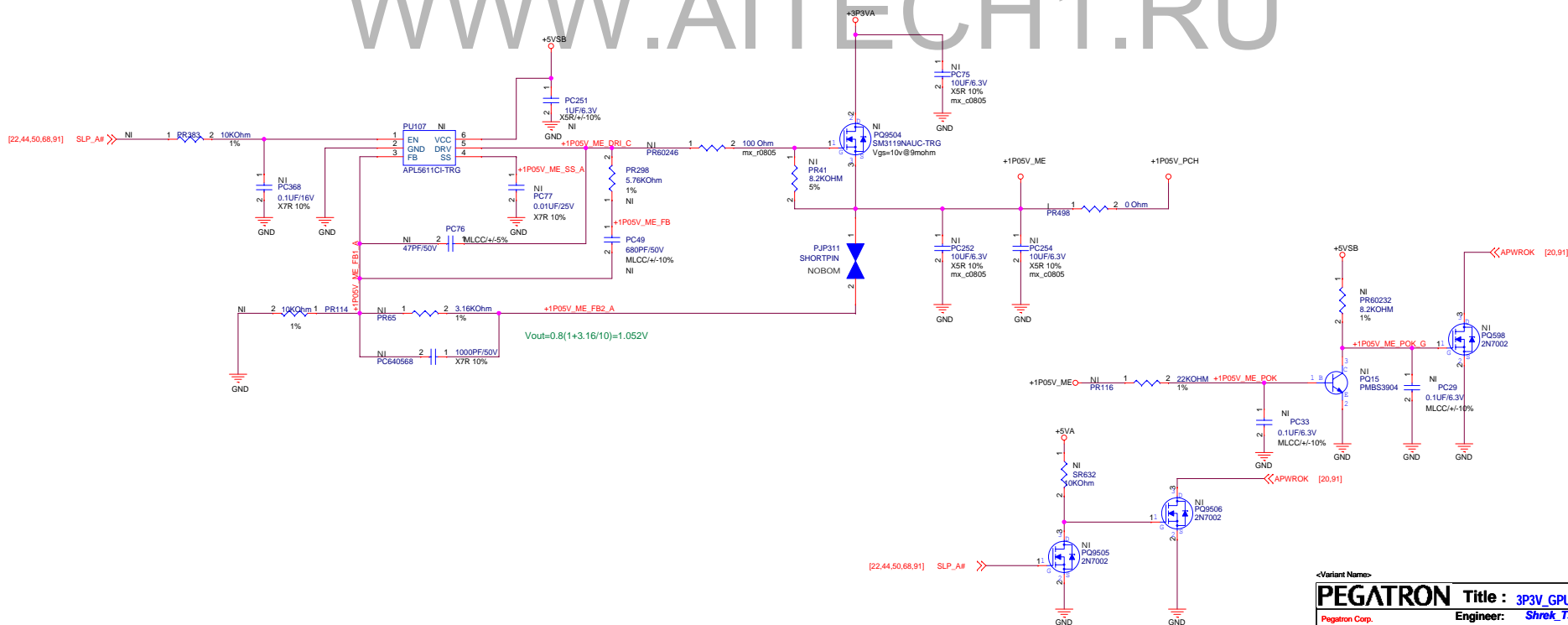


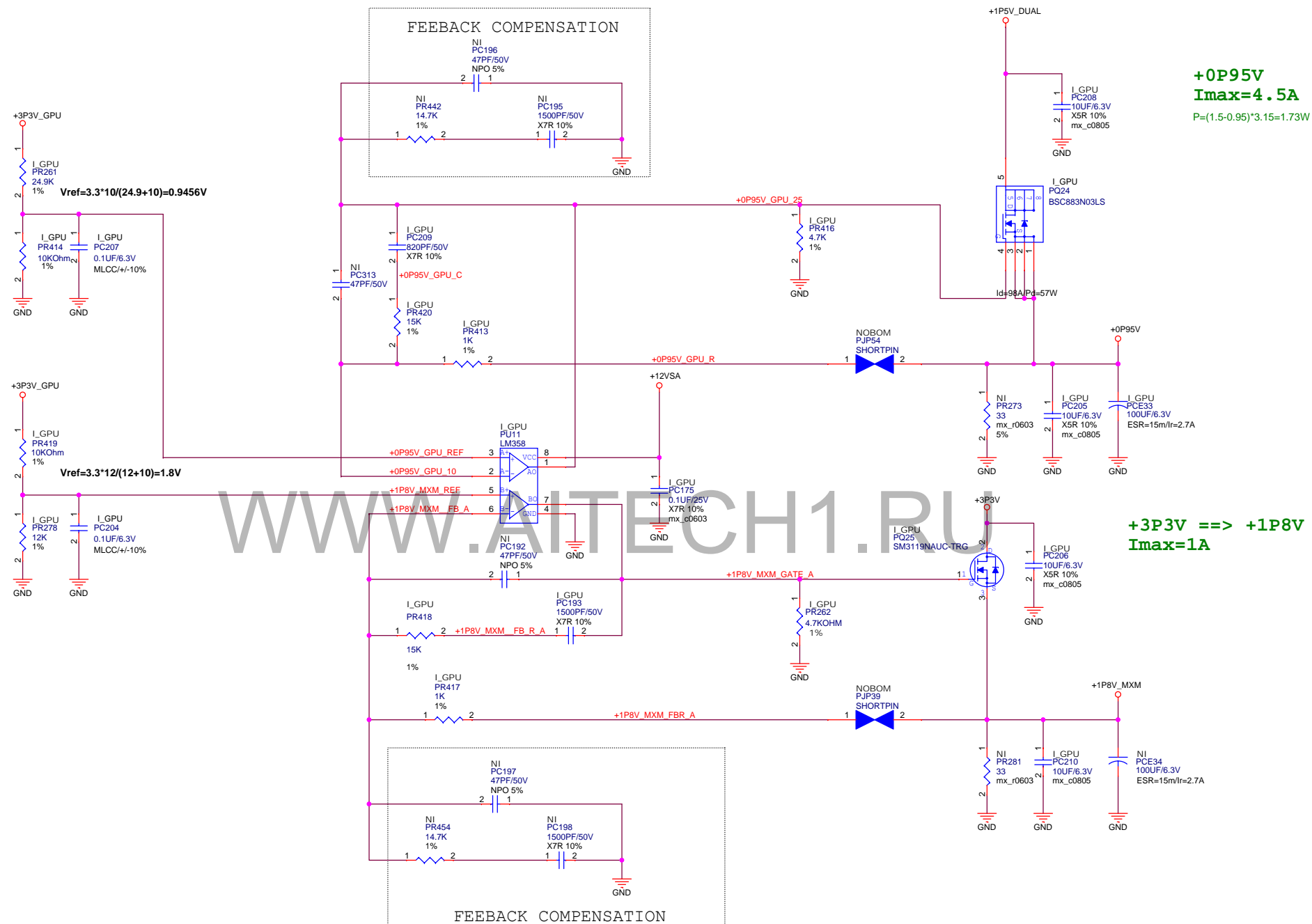
+1P5V_GPU
IMAX=8A
Trace Width>240mil



WWW.AITECH1.RU

+1P05V_ME/Imax:1A
 $P_d = 0.55' (3.3 \cdot 1.05) = 1.2W$





+0P95V
Imax=4.5A
 $P=(1.5-0.95)*3.15=1.73W$

+3P3V ==> +1P8V
Imax=1A

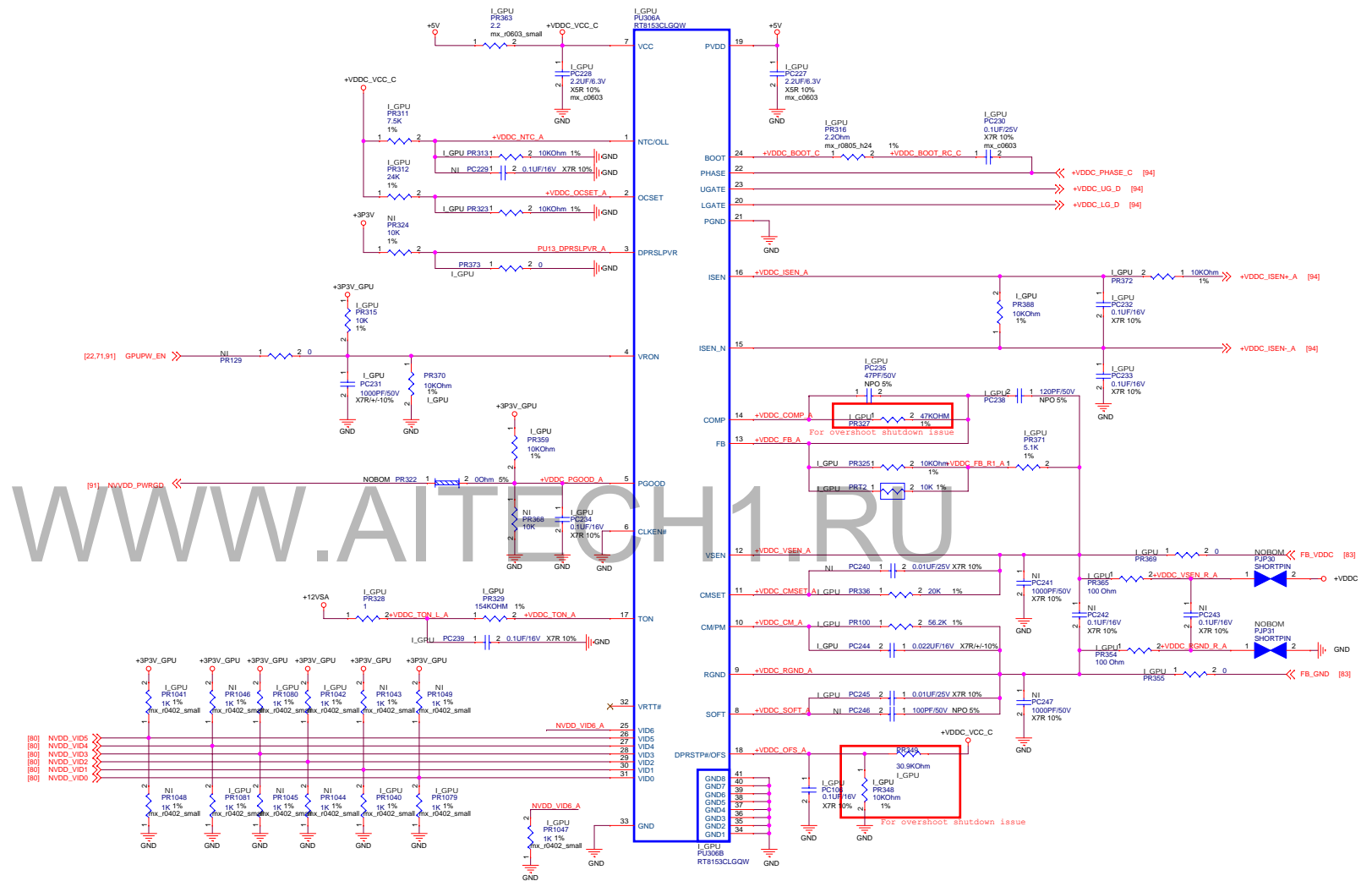
PEGATRON DT-MB RESTRICTED SECRET

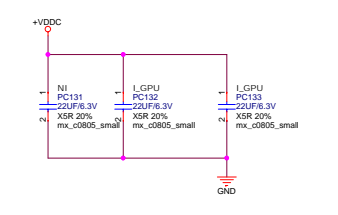
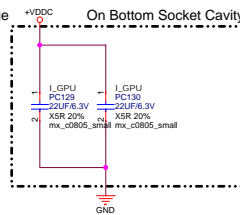
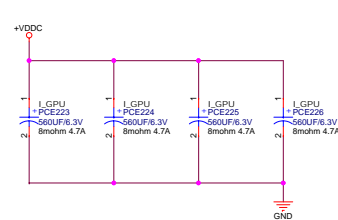
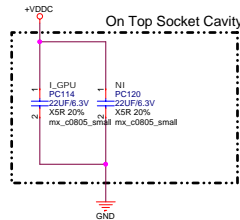
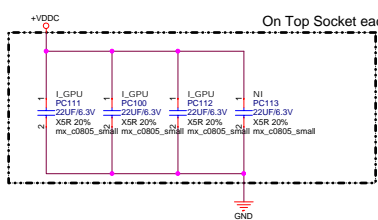
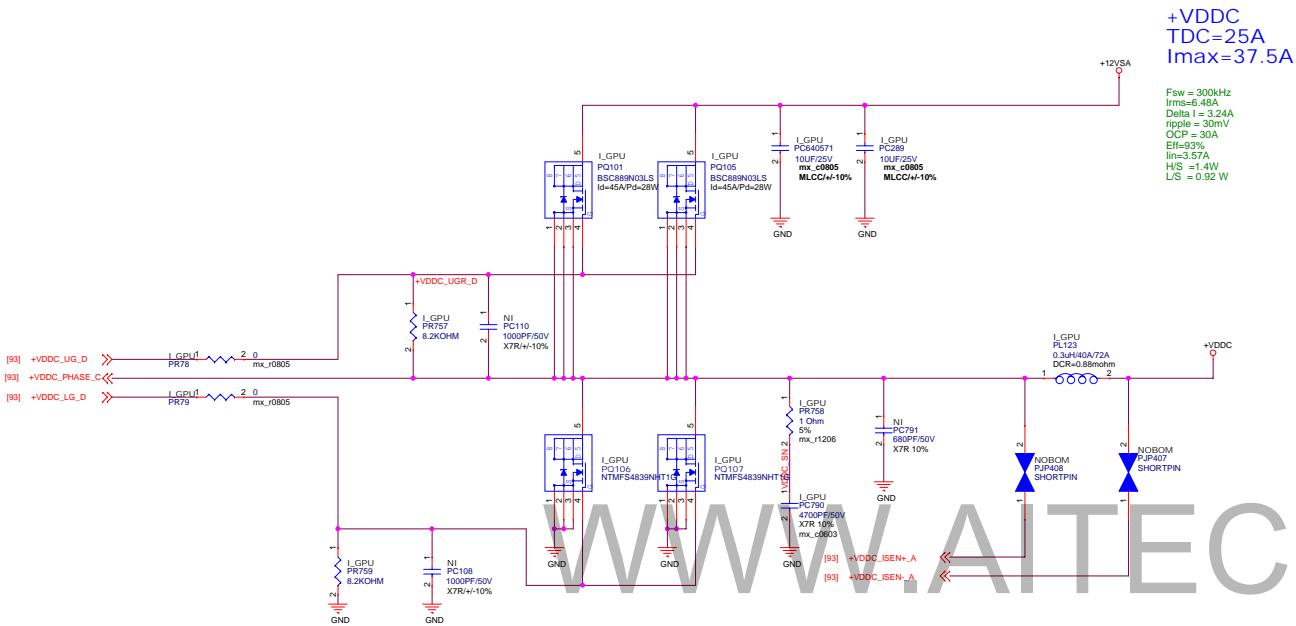
PEGATRON Title : +0P95V & +1P8V_MXM

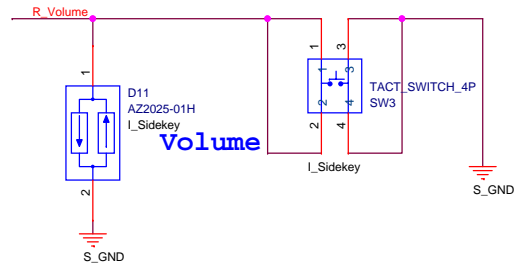
Pegatron Corp. Engineer: Shrek Tseng

Size A3 Project Name IPPLP-TH

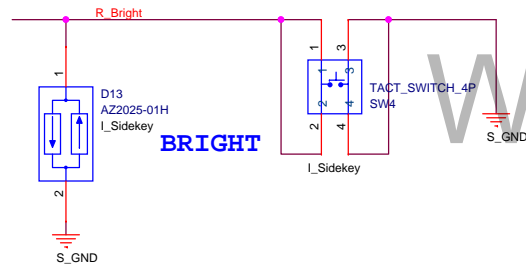
Date: Friday, January 17, 2014 Sheet 92 of 97



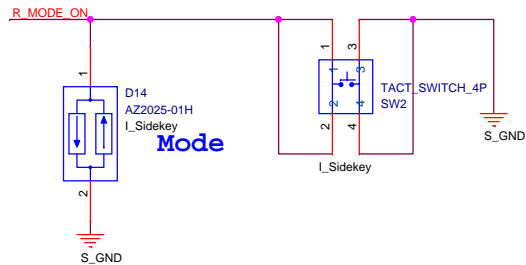




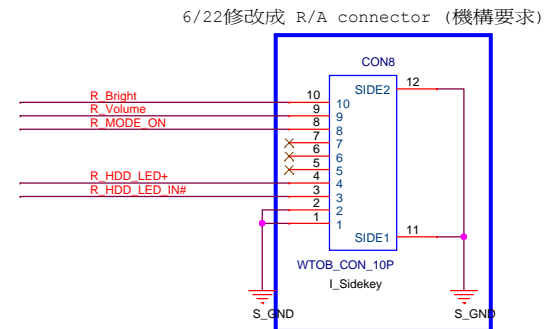
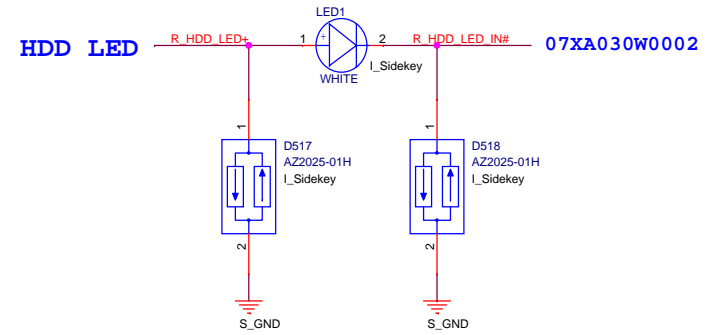
HF P/N: 12X902050B30
1209-008C000
1209-007V000



HF P/N: 12X902050B30
1209-008C000
1209-007V000



HF P/N: 12X902050B30
1209-008C000
1209-007V000



PPID1

40X4_WHITE

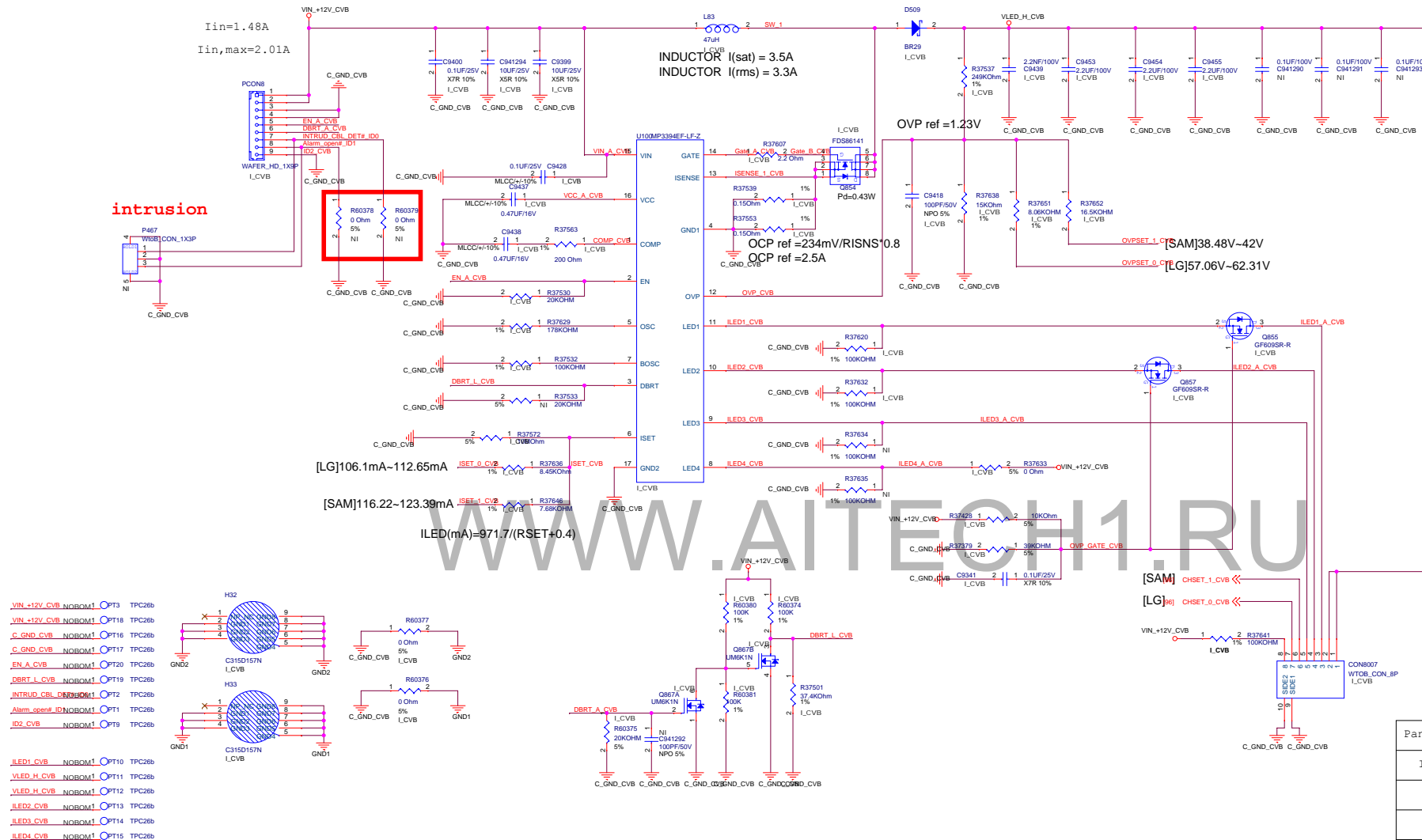
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIDE KEY

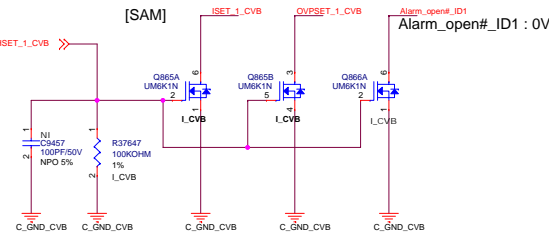
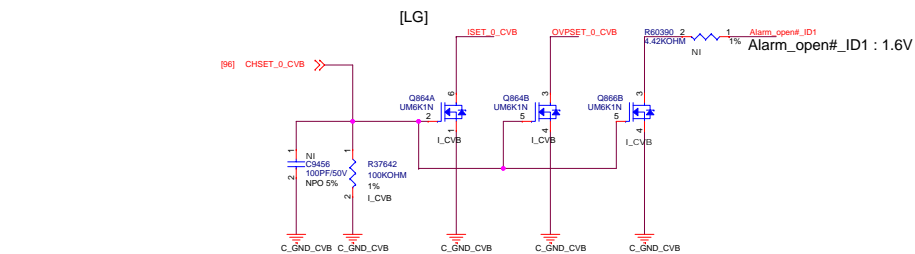
Pegatron Corp. Engineer: Shrek Tseng

Size A3 Project Name IPPLP-TH Rev A00

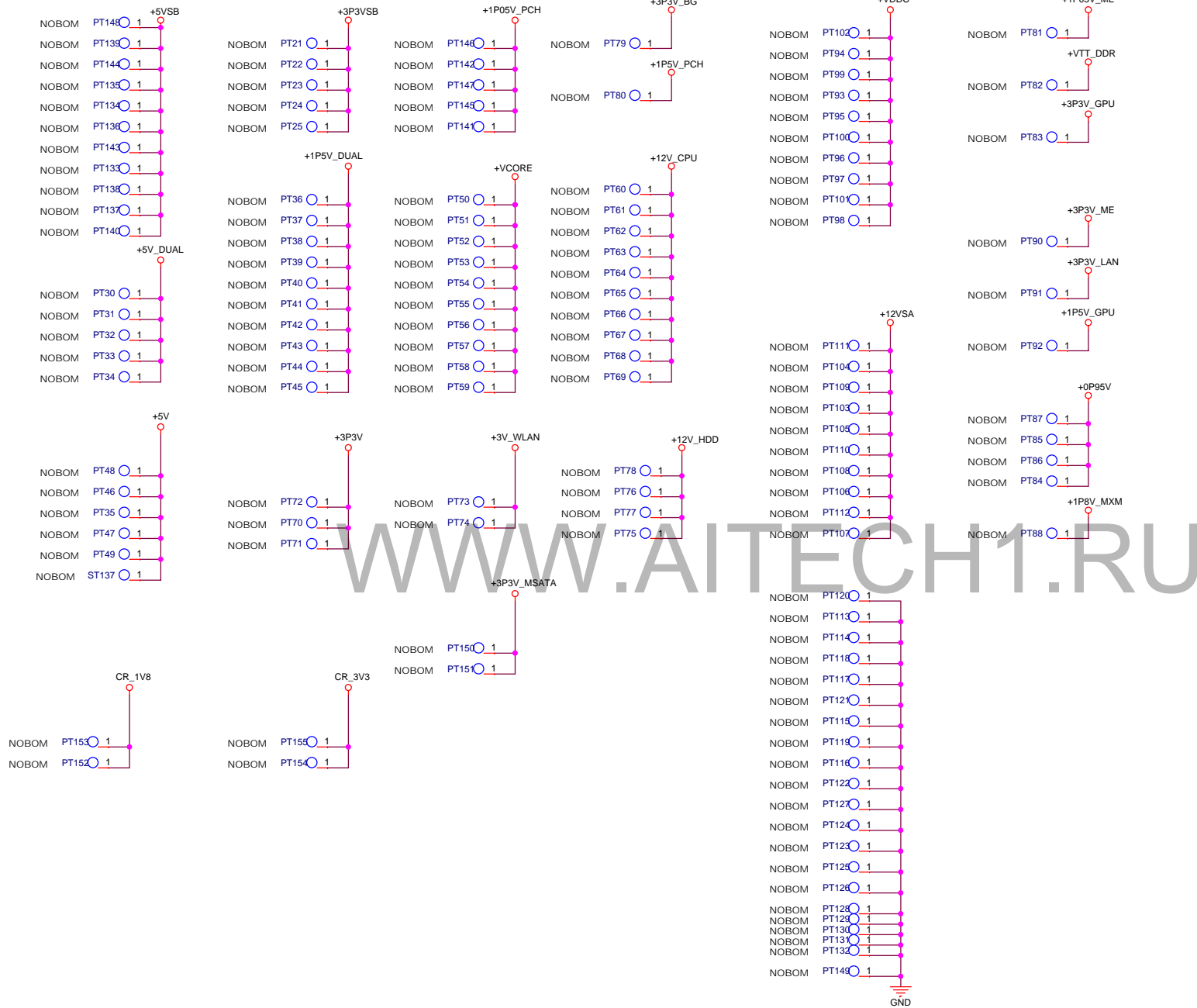
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- VIN+12V_CVB NOBOM1 OPT3 TPC26b
- VIN+12V_CVB NOBOM1 OPT18 TPC26b
- C_GND_CVB NOBOM1 OPT16 TPC26b
- C_GND_CVB NOBOM1 OPT17 TPC26b
- EN_A_CVB NOBOM1 OPT20 TPC26b
- DBRT_L_CVB NOBOM1 OPT19 TPC26b
- INTRUD_CBL NOBOM1 OPT2 TPC26b
- Alarm_open#_ID NOBOM1 OPT1 TPC26b
- ID2_CVB NOBOM1 OPT9 TPC26b
- ILED1_CVB NOBOM1 OPT10 TPC26b
- VLED_H_CVB NOBOM1 OPT11 TPC26b
- VLED_H_CVB NOBOM1 OPT12 TPC26b
- ILED2_CVB NOBOM1 OPT13 TPC26b
- ILED3_CVB NOBOM1 OPT14 TPC26b
- ILED4_CVB NOBOM1 OPT15 TPC26b



Panel (23")	LG	SAM
ILED.typ	110/120 mA	120/130 mA
VF	52.7/56.1V	34/37V
OVP	59.64V	40.21V
Pin NO.	4	4
ID	1 1	1 0
ID Level (V)	1.6	0



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : TP

Pegatron Corp. Engineer: Shrek_Tseng

Size A3 Project Name IPPLP-TH Rev A00

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